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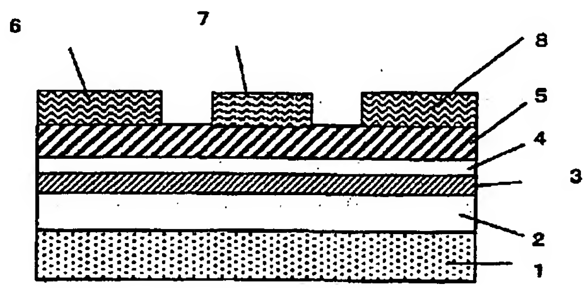
(54)【発明の名称】　半導体装置

(57)【要約】　（修正有）

【課題】　ＧａＮ系電界効果トランジスタにおいて、ＧａＮのバッファー層中の残留キャリアの伝導によるリーク電流成分を低減しトランジスタのピンチオフ特性を向上させる。

【解決手段】　ＧａＮバッファー層と、ＧａＮあるいはＩｎＧａＮとＧａＮを組み合わせたチャンネル層と、ＡｌＧａＮ層とがサファイア基板あるいはＳｉＣ基板上に順次形成されたヘテロ構造のＧａＮバッファー層中にＡｌＧａＮ層を設け、設けられたＡｌＧａＮ層におけるＡｌＮ組成比を表面のＡｌＧａＮ層のＡｌＮ組成比よりも小さくする。



【特許請求の範囲】

【請求項1】　GaNバッファー層と、第一のAlGaN層と、GaNあるいはInGaNとGaNを組み合わせたチャンネル層と、第二のAlGaN層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの層の表面がIII族原子のc面となるヘテロ構造を用いた半導体装置であって、

該第一のAlGaN層におけるAlN組成比が該第一のAlGaN層におけるAlN組成比よりも小さいことを特徴とする半導体装置。

【請求項2】　前記第一のAlGaN層におけるAlN組成比が0．1以下であることを特徴とする請求項1に記載の半導体装置。

【請求項3】　前記第一のAlGaN層の組成比が基板側から表面側へ次第に高くなるように設定したことを特徴とする請求項1に記載の半導体装置。

【請求項4】　GaNバッファー層と、$(In_xAl_{1-x})_yGa_{1-y}N$層と、GaN、InGaNあるいはInGaNとGaNを組み合わせたチャンネル層と、AlGaN層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの表面がIII族原子のc面となるヘテロ構造を用いた半導体装置であって、

該$(In_xAl_{1-x})_yGa_{1-y}N$層と該チャンネル層とのヘテロ界面において分極の変化に基づき電子の蓄積が生じるように該$(In_xAl_{1-x})_yGa_{1-y}N$層のAlN組成比、InN組成比、GaN組成比が設定されたことを特徴とする半導体装置。

【請求項5】　GaNバッファー層と、AlGaN層と、GaN、InGaNあるいはInGaNとGaNを組み合わせたチャンネル層と、$(In_xAl_{1-x})_yGa_{1-y}N$層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの表面がV族原子のc面となるヘテロ構造を用いた半導体装置であって、

該$(In_xAl_{1-x})_yGa_{1-y}N$層と該チャンネル層とのヘテロ界面において分極の変化に基づき電子の蓄積が生じるように該$(In_xAl_{1-x})_yGa_{1-y}N$層のAlN組成比、InN組成比、GaN組成比が設定されたことを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置に関し、特に$(In_xAl_{1-x})_yGa_{1-y}N$（$0\leq X\leq 1$、$0\leq Y\leq 1$）で表される窒化ガリウム系半導体のヘテロ構造を用いた電界効果トランジスタ等の半導体装置に関するものである。

【0002】

【従来の技術】GaN、AlGaN、InGaN、InAlGaN等の窒化ガリウム系半導体は高い絶縁破壊電界強度、高い熱伝導率、高い電子飽和速度を有しており、高周波のパワーデバイス材料として有望である。特に、AlGaN／GaNヘテロ接合構造ではAlGaNとGaNとのヘテロ接合界面付近に電子が高濃度で蓄積し、いわゆる二次元電子ガスが形成され、この二次元電子ガスがAlGaNに添加されるドナー不純物とは空間的に分離されて存在するため高い移動度を示す。従って、電界効果型トランジスタにこのヘテロ構造を用いると、ソース抵抗成分を低減することができる。しかも、ゲート電極から二次元電子ガスまでの距離dは通常数十nmと短いため、ゲート長Lgが100nm程度と短い場合でも、アスペクト比Lg／dは5から10と大きくできる。その結果、AlGaN／GaNヘテロ構造を用いることにより、短チャネル効果の小さい良好な飽和特性を有する電界効果型トランジスタを容易に作製できるという優れた特徴を有する。さらにAlGaN／GaN系ヘテロ構造における二次元電子は、1×10^5V／cm程度の高電界領域で、高周波トランジスタとして普及しているAlGaAs／InGaAs系の場合に比べて2倍以上の電子速度を有しているために、このようなヘテロ構造は、高周波のパワーデバイスへの応用が期待されている。

【0003】図8にAlGaN／GaN系ヘテロ構造を有するFETの断面図の一例を示す。このFETのAlGaN／GaN系ヘテロ構造は、通常［0001］面（c面）のサファイア基板、SiC基板等の基板1上に、有機金属気相成長法や分子線エピタキシー法を用いて結晶成長される。図8では、サファイア基板またはSiC基板1の上にGaNバッファー層2、AlGaN層5が順次積層され、AlGaN層5上に、ソース電極6、ゲート電極7、ドレイン電極8がそれぞれ分離して形成される。サファイア基板、SiC基板上の何れにおいてもGaNと基板の格子定数は大きく異なるので、これら基板に厚く形成されたGaNバッファー層2は格子不整に基づく歪が十分緩和した状態で形成される。この厚いGaNバッファー層2の上にSiなどのn型不純物を添加したAlGaN層5を数十nmの厚さに形成すると、選択ドーピングの効果によりヘテロ界面において電子親和力の大きいGaNバッファー層2の方に二次元電子ガスが形成される。MOCVD（有機金属気相成長）法で形成されたヘテロ構造においては、結晶表面は通常、III族原子Gaの面であり、この二次元電子ガスの濃度はAlGaN層5とGaNバッファー層2の自発分極の差およびAlGaN層5が受ける引っ張り応力によるc軸方向のピエゾ分極の効果が加わり、AlGaN層5に添加したn型不純物の濃度から予測される値よりも高濃度の電子が蓄積することが知られている。その濃度は、AlGaN層5のAl組成が0．2から0．3の場合に1×10^{13}／cm^2程度でありGaAs系デバイスの約3倍に達する。このような高濃度の二次元電子ガ

スが蓄積されることから、GaN系ヘテロ構造FETはパワーデバイスとして非常に有望視されているが、改善すべき問題点も多くある。

【0004】

【発明が解決しようとする課題】GaN系ヘテロ構造FETにおける第一の問題点は、結晶成長技術が未熟なため品質の良好な結晶が得られていないことである。結晶成長に関する問題のひとつに、ノンドープのGaNが通常n型を示し、キャリア濃度も10^{16}/cm^3程度あるいはそれ以上と高いことである。これは、結晶成長時に構成元素である窒素(N)が抜け、窒素の空孔ができやすいことが原因であるとされている。このような残留のキャリアがあると素子のGaNバッファー層2を介してのリーク電流成分が大きくなり、特に高温で動作させた場合にピンチオフ特性が悪くなるなど、素子特性の劣化につながることになる。また複数のGaN系ヘテロ構造のFETを同一の基板に形成した場合にFET同士が互いに干渉しあい、正常な動作が妨げられるという素子分離についての問題も生じる。さらにゲート電極がこのGaN層バッファー層2上に設けられた場合には、ゲートリーク電流が増大するという問題も発生する。

【0005】GaN系ヘテロ構造FETにおける第二の問題点は、すでに述べた分極の効果に起因するものである。従来用いられているAlGaAs/InGaAs系ヘテロ構造FETでは、チャンネル層としてInGaAsを用い、キャリア供給層にSiを添加したAlGaAsを用いる。パワーデバイスに用いる際には、チャンネル層のInGaAs層を二つのn型AlGaAs層で挟んだAlGaAs/InGaAs/AlGaAsという構造にし、チャンネルの電子濃度を2倍程度に高めた構造が用いられる。図9に、深さ方向の伝導体ポテンシャルエネルギーの形状を示す。図9から分かるように、中央のポテンシャルの低いInGaAs層に両側のAlGaAs層から電子が供給されることになる。Siを添加したAlGaAsが二つあるのでこのような構造はダブルドープ構造あるいはダブルドープダブルヘテロ構造と呼ばれる。

【0006】一方、GaN系で図9と同様なダブルドープ構造、すなわちn型AlGaN/GaN/n型AlGaNを形成した場合の構造を図10に、また深さ方向の伝導体ポテンシャルエネルギーの形状を図11に示す。図10では、サファイア基板またはSiC基板1の上に、GaNバッファー層2、AlGaN層13、GaN層4、およびAlGaN層5が順次積層され、AlGaN層5上に、ソース電極6、ゲート電極7およびドレイン電極8がそれぞれ分離して形成される。図10に示されるGaN系のダブルドープ構造では、チャンネル(下記で述べる)に供給される電子は、分極の効果による影響が大きいので、ここではドーピングは表面側のAlGaN層5のみにおこなっている。図11のグラフから分かるように、この系の場合はピエゾ分極や自発分極のヘテロ界面での不連続の効果が大きく発現するため電子の蓄積する領域が二つに完全に分かれ、AlGaN層5とGaN層4とのヘテロ界面に形成される表面側の第一のチャンネル、および、基板側の電子供給層であるAlGaN層13とGaNバッファー層2とのヘテロ界面に形成される基板側の第二のチャンネルを電子が流れることになる。これら二つのチャンネルの距離は数十nm以上と大きく、FETの相互コンダクタンスはAlGaAs/InGaAs/AlGaAsのようにひとつのチャンネルに電子が溜まる場合に比較して小さくなる。このためFETの利得は小さくなり高周波動作の観点からは好ましくない。

【0007】本発明は、以上に述べたようなGaN系ヘテロ構造FETの問題点に鑑みなされたものであり、その第一の目的は、GaN層中の意図せず導入される残留キャリアによるソース・ドレイン間リーク電流の増大、ゲートリーク電流の増大、素子間リーク電流の増大を改善することができる半導体装置を提供することにある。本発明の第二の目的は、ひとつのチャンネル層に電子を蓄積できる新たな構造を用いることにより、高い相互コンダクタンスと高い電流駆動能力を有するダブルドープ型のGaN系ヘテロ構造の半導体装置を提供することにある。

【0008】

【課題を解決するための手段】図10を参照して説明したように、単にGaNバッファー層にAlGaNの薄層を設けるのでは2つの互いに分離した電子チャンネルが形成され基板側のチャンネルにも多量の電子が蓄積され、しかもこの電子はドレイン電流を増加させることに大きく寄与しない。従って、電界効果トランジスタのゲートの容量を増加させるだけでトランジスタの性能をかえって低下させることにつながる。しかしながら、図10で設けされたAlGaN層13とその上のGaN層4とのヘテロ界面での分極の不連続によるポテンシャルの引き上げ効果については、表面側の電子を表面側のチャンネルに閉じ込める働きがあるので、トランジスタのドレインコンダクタンスを低下させトランジスタの電力利得を向上させたり、ゲート長を短縮しやすいので動作周波数を向上させることができるものと期待される。

【0009】本発明の半導体装置の実施形態は、こうしたポテンシャルの引き上げ効果を利用し、且つ、形成されたAlGaN層とGaNバッファー層のヘテロ界面には殆ど電子を蓄積しないように、AlGaN層のAlN組成比を表面のAlGaN層におけるAlN組成比よりも大幅に小さくすることを特徴とし、さらに設けられるAlGaN層の層厚を従来例にくらべ十分厚く形成するものである。

【0010】本発明の半導体装置の別の実施形態は、設けられる層をAlGaNではなく分極の不連続値がAl

GaNの場合と反対符号となる$(In_xAl_{1-x})_yGa_{1-y}N$層を用いる。これにより分離した二つのチャンネルのうち基板側のチャンネルは消滅し、すべての電子が表面側のチャンネルに蓄積するようになり、AlGaAs　InGaAs／AlGaAs系の選択ドープダブルヘテロ構造と類似したポテンシャル形状を得ることができる、すなわち$(In_xAl_{1-x})_yGa_{1-y}N$層のxおよびyの値を適切に設定することで、この層を表面側チャンネルへの電子供給層として用いることが可能となる。この構成を用いる場合は、当然のことながらチャンネルを実質的にひとつにすることを目的とするので、$(In_xAl_{1-x})_yGa_{1-y}N$層上のGaN、InGaNあるいはInGaNとGaNを組み合わせたチャンネル層の厚さを10〜20nmと薄くすることが重要である。

【0011】以下に本発明の手段についてより具体的に説明する。

【0012】本発明による半導体装置は、GaNバッファー層と、第一のAlGaN層と、GaNあるいはInGaNとGaNを組み合わせたチャンネル層と、第二のAlGaN層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの層の表面がIII族原子のc面となるヘテロ構造を用いた半導体装置であって、前記第一のAlGaN層におけるAlN組成比が前記第一のAlGaN層におけるAlN組成比よりも小さいことを特徴とすることにより、上記目的が達成される。

【0013】前記第一のAlGaN層におけるAlN組成比が0．1以下であってもよい。

【0014】前記第一のAlGaN層の組成比が基板側から表面側へ次第に高くなるように設定してもよい。

【0015】本発明による半導体装置は、GaNバッファー層と、$(In_xAl_{1-x})_yGa_{1-y}N$層と、GaN、InGaNあるいはInGaNとGaNを組み合わせたチャンネル層と、AlGaN層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの表面がIII族原子のc面となるヘテロ構造を用いた半導体装置であって、前記$(In_xAl_{1-x})_yGa_{1-y}N$層と前記チャンネル層とのヘテロ界面において分極の変化に基づき電子の蓄積が生じるように前記$(In_xAl_{1-x})_yGa_{1-y}N$層のAlN組成比、InN組成比、GaN組成比が設定されたことを特徴とすることにより、上記目的が達成される。

【0016】本発明によるGaNバッファー層と、AlGaN層と、GaN、InGaNあるいはInGaNとGaNを組み合わせたチャンネル層と、$(In_xAl_{1-x})_yGa_{1-y}N$層とが、サファイア基板あるいはSiC基板上に順次形成された構造を有し、かつそれぞれの表面がV族原子のc面となるヘテロ構造を用いた半導体装置であって、前記$(In_xAl_{1-x})_yGa_{1-y}N$層と前記チャンネル層とのヘテロ界面において分極の変化に基づき電子の蓄積が生じるように前記$(In_xAl_{1-x})_yGa_{1-y}N$層のAlN組成比、InN組成比、GaN組成比が設定されることを特徴とすることにより、上記目的が達成される。

【0017】

【発明の実施の形態】（実施形態1）本発明の実施形態1に係る半導体装置を図面に基づいて説明する。図1aは、本発明の実施形態1に係る半導体装置である電界効果型トランジスタ（FET）の断面図、図1bはゲート電圧が0Vの場合の、深さ方向に見た伝導帯ポテンシャルエネルギーの形状を示す一例である。

【0018】MOCVD法を用いてサファイア基板1の上にまずGaN（層厚約20nm）と、その上にノンドープのGaN（層厚2μm）をバッファー層2として成長させる。次に、AlNの組成比を0．1以下、より好ましくは0．01〜0．05の範囲の低AlN組成のAlGaN分離層3（層厚が50〜300nm）を形成し、さらにGaN層4（層厚300〜500nm）をチャンネル層4として形成する。次に、このGaNチャンネル層4上にSiをドープしたキャリア濃度を例えば$2\times10^{18}cm^{-3}$のn型AlGaN電子供給層5（層厚20nm）に形成する。AlGaN電子供給層5の上には、ソース電極6、ゲート電極7、ドレイン電極8がそれぞれ分離して形成される。

【0019】図1bに、AlN組成が0．01の低AlN組成の分離層3を約200nmの厚さに、その上のGaN層4を約300nmの厚さに、n型AlGaN電子供給層5を20nmの厚さにそれぞれ設定した場合のポテンシャルプロファイルを示す。この場合、分離層3とGaN層4との和である空乏層は、約500nmの厚さとなり、ポテンシャルのピーク値は1eVに達する。基板1側のヘテロ界面のポテンシャルはフェルミレベル（ポテンシャルが0eVのレベル）よりも高く、この界面の電子濃度は$10^{11}/cm^2$のオーダーであり十分に低い。しかも厚い空乏層により表面のチャンネルと完全に分離されている。

【0020】このようなFETの構造は、従来のFETの構造（図8）と比較した場合、低AlN組成のAlGaN分離層3が設けられている点で異なる。この分離層3を設けることにより、キャリア濃度およびその温度依存性が大きく向上する。

【0021】図2は、従来のGaNバッファー層のみのヘテロ構造を有するFETと、GaN層中に低AlN組成のAlGaN分離層3を設けた本発明のFETの基板におけるホール測定によるシート電子濃度の温度変化を示す。低AlN組成のAlGaN分離層3を設けた本実施形態FETでは、電子濃度が高い温度でやや増加するものの、室温から77K付近までほぼ一定の値を示すことがわかる。この一定の電子濃度はAlGaN電子供給層5とその下のGaNバッファー層4とのヘテロ界面に

蓄積する二次元電子ガスの濃度に対応すると考えられる。一方、低AlN組成のAlGaN分離層3のない従来のFET構造では、より高い電子濃度を示し、且つ、その温度依存性も大きい。電子濃度が温度により増加するのはGaNバッファー層2中のドナーのイオン化に起因すると考えられ、低AlN組成のAlGaN分離層3のない場合にはGaNの全バッファー層2中の電子濃度が測定されるのに対し、分離層3を設けることによってオーミック電極がこの高抵抗の空乏層を突き抜けず、GaNバッファー層2においてイオンの発生が減少した結果、低AlN組成のAlGaN分離層3より下のバッファー層2中の電子濃度が測定されなくなったものと推察できる。

【0022】従来のFETの構造と本発明の実施形態1によるFET構造の代表的な静特性を、それぞれ図3a、図3bに示す。低AlN組成のAlGaNの分離層3を設けた本発明の構造ではFETのピンチオフ特性が良好であり、ゲート電圧が−4V付近でドレイン電流が流れなくなるが、従来のGaNバッファー層のみのFETの場合は、ドレイン電流が遮断されずリーク電流として流れ続けていることがわかる。このようなリーク電流の大きい素子では、複数の素子を同一基板に形成し集積回路を作製した場合、素子同士が互いに干渉し合い正常に動作しなくなるという問題が生じる。また無効な電流成分が大きくなるためパワーデバイスの効率の低下、高周波動作の劣化が生じる。

【0023】以上のように、本発明の実施形態1によるFETは、GaNバッファー層2とGaNチャンネル層4との間に低AlN組成のAlGaN分離層3を導入することによってGaNバッファー層中に意図せず導入される残留キャリアによるソース・ドレイン間リーク電流の増大、ゲートリーク電流の増大、素子間リーク電流の増大を効果的に低減でき、高周波パワーデバイスの特性向上、それらの集積回路の異常動作の防止に大いに貢献できるものである。

【0024】ここでAlGaNによる分離層3がGaNバッファー層2とGaNチャンネル層4との間にどのように設けられるべきかについて考察を行う。従来、AlGaNの薄層を導入することは本発明と異なる意味合いでなされてきた。図10および図11を参照して説明した従来例も、AlGaNの薄層が設けられるという点で同じあるが、本発明において設けられるAlGaN分離層3のAlN組成比および位置とははっきり異なる。

【0025】文献としてはJournal of Applied Physics vol. 85 (1999) pp. 3009-3011に記載のR. Gaska達の報告している同様なダブルチャンネルのヘテロ構造FETがある。このFETの構造はサファイア基板に50nmの厚さのAlGaN、800nmの厚さのGaN層、25nmの厚さのAlGaN層、100nmのGaNチャンネル層、30nmの厚さのAlGaNバリア層が順次形成されたものであり、この中で25nmのAlGaN層は本発明のFETにおけるAlGaN分離層と同じように見えるが、このFETでは、その論文の題目「Two-channel AlGaN/GaN heterostructure field effect transistor for high power applications」からも分かるとおり、二つのチャンネルを形成することが目的である。そのためGaNチャンネル層は100nmと薄く、基板側のチャンネル層までの基板表面からの距離は150nmと短い。また、このFETでは、設けられるAlGaN層のAlN組成が表面側と同じであるので、その厚さを厚くできない。その理由は、GaNチャンネル層との格子不整合に伴うAlGaN分離層の臨界膜厚による制限をうけること、および、設けられるAlGaN層を厚くした場合にポテンシャルの引き上げ効果が大きくなりすぎて設けられたAlGaN層と表面側のGaN層とのヘテロ界面に正孔が蓄積されることである。この正孔濃度がある程度高くなると、ゲート電圧の変化による正孔濃度の変化に起因するゲート容量が無視できなくなりFETの高周波特性が劣化する。高周波特性を向上させるためには正孔蓄積を防止するか蓄積する箇所を表面からできるだけ遠ざけ、ゲート電圧やドレイン電圧の変動による電荷量の変化をできるかぎり低減することが重要となる。

【0026】本発明の実施形態1における第一の特徴は、AlGaN分離層3のAlN組成比を表面側のAlGaN層5の値よりも十分低くし、低AlN組成のAlGaN分離層3とGaNバッファー層2とのヘテロ界面にほとんど電子の蓄積が見られないようにすることである。第二の特徴は、低AlN組成のAlGaN分離層3の厚さを増し、これによって所望のポテンシャル引き上げ効果を得ることである。第三の特徴は、低AlN組成のAlGaN分離層3を表面から十分離れたところに設けるものであり、あくまでひとつのチャンネルを有する素子とすることである。このような構成において重要となるのは、GaNチャンネル層4の厚さを厚くしすぎないことである。

【0027】GaNチャンネル層4の適切な厚さを以下に大まかに見積もる。この層に意図せず導入されるドナー濃度に基づく余分のキャリアの濃度として許される範囲は、飽和2次元電子ガス濃度の1/50〜1/100以下と考えられる。その場合、シートキャリア濃度はおよそ$1〜3×10^{11}/cm^2$である。残留ドナー濃度として$1×10^{16}/cm^3$を仮定し、ピークポテンシャルとしてGaNのバンドギャップ3.2eVを考慮して、2eVまでと設定すると空乏化するGaNチャンネル層4の厚さは460nmである。残留ドナー濃度を$5×10^{16}/cm^3$と仮定した場合は、GaNチャンネル層4

の厚さは約205nmである。これらの層厚に常識的に考えられるチャンネルの層厚(50nmから100nm)を加えると、およそ250nmから560nmの範囲が適当であると考えられる。

【0028】以上からGaNチャンネル層4の適切な厚さとして300〜500nmが見積もれる。この深さは通常の典型的なオーミック電極形成条件において電極金属が浸入する深さ(100nm以下)よりも十分深く、さらにGaNチャンネル層4の下に低AlN組成のAlGaN分離層3が存在するので電流はGaNバッファー層2を流れることはない。また、低AlN組成のAlGaN分離層3とその下のGaNバッファー層2とのヘテロ界面には極薄い濃度の2次元ガスが溜まるだけであるので、ゲート容量が著しく増大することもなく、電界効果トランジスタの高周波特性を損なうことがない。

【0029】(実施形態2)本発明の実施形態2のFETは、実施形態1における低AlN組成のAlGaN分離層3をAlN組成が基板側から表面側へ徐々に増加させる構成となっている。具体的には、AlNの組成比を例えば0から0.05まで成長方向、すなわち表面側へ増加させ、層厚として例えば100nm〜300nmとなるように形成する。表面側へ向かっての組成の変化率は正であればよく、特に限定する理由はない。このように低AlN組成のAlGaN分離層3とその下のGaNバッファー層2のヘテロ界面をなだらかにすることにより、この部分にたまる電子の濃度を低下させることが可能となり、ゲート容量を低減できる。

【0030】(実施形態3)本発明の実施形態3のFETについて図4を用いて説明する。図4に示すFETは、実施形態1に関する図1aに示すFETのチャンネル層4をGaN層41とInGaN層42の二層構造としたものである。このような構造はInGaN層42をAlGaN層5とGaN層4の間に設けることで実現される。よりエネルギーバンドギャップの小さいInGaN層42をチャンネルに用いることにより、チャンネルに溜まる電子濃度を高め、InGaN層42に電子を実質的に閉じ込め、ゲート長の短縮をより容易に実現する。実際には、図4におけるInGaN層41以外は、実施形態1のFETの層構造とまったく同一であってよい。InGaN層42におけるInNの組成は0.05〜0.2程度の範囲が適切であり、その層厚は10nmから20nmの範囲が適当である。

【0031】(実施形態4)本発明の実施形態4に係る半導体装置を図5に基づいて説明する。図5は実施形態4に係る電界効果型トランジスタ(FET)の断面図である。

【0032】前述したように、GaN層に薄いAlGaN層を設けて二つのチャンネルを形成する従来の構造では、自発分極とピエゾ分極の効果により設けたAlGaN層の上下二つのヘテロ界面に正孔あるいは電子の蓄積が生じやすく、電子が流れる二つのチャンネルも数十nmという大きな距離を隔てて形成されるため、デバイスのピンチオフ特性が良くないこと、余分の容量が付加され高周波特性が劣化するという問題が生じる。図5に示すFETでは、従来の問題点を解決する新しいヘテロ構造を提供するものであり、薄いAlGaN層の代わりに$(In_xAl_{1-x})_yGa_{1-y}N$を用いる。

【0033】具体的構造として、図5に示すように、MOCVD法を用いてサファイアまたはSiC基板1の上にまずGaNのバッファー層2(層厚約2μm)を成長させる。次に、$(In_xAl_{1-x})_yGa_{1-y}N$層31(層厚約10nmから30nm)を成長させる。この$(In_xAl_{1-x})_yGa_{1-y}N$層31は通常Siなどのn型不純物が添加され、その濃度は$1〜5x10^{18}/cm^3$のオーダーである。層厚は主にこの層に導入される圧縮歪により規定される臨界層厚程度に薄くする必要がある。この$(In_xAl_{1-x})_yGa_{1-y}N$層31上にチャンネル層43を形成する。このチャンネル層43はGaN層単独でもよいし、InGaN層単独あるいはGaN層とInGaN層の組み合わせでもよい。ただしチャンネル層全体の層厚は10nmから30nm程度に薄く形成することがFETの相互コンダクタンスを低下させない上で重要である。InGaN層をチャンネル層43に用いる場合は、実施形態3で述べたように、InNの組成を0.05〜0.2程度の範囲とし、層厚としては10nmから20nmの範囲が適当である。チャンネル層43の上にはn型のAlGaN電子供給層5が形成される。そのAlN組成は0.15〜0.5、層厚は10〜30nm、n型不純物濃度は$1〜5x10^{18}/cm^3$の範囲が適切である。AlGaN電子供給層5の上には、ソース電極6、ゲート電極7、ドレイン電極8がそれぞれ分離して形成される。

【0034】図6において、チャンネル層43がGaN層よりなる場合の上記ヘテロ構造中の深さ方向のポテンシャル形状を示す。$(In_xAl_{1-x})_yGa_{1-y}N$層31を用いることによって、電子を表面側のチャンネル層のみに蓄積することが可能となり、図9で示したAlGaAs/InGaAs/AlGaAs構造と類似したポテンシャル形状が得られる。その結果$(In_xAl_{1-x})_yGa_{1-y}N$層31とAlGaN層5の両側から電子が供給され、$(In_xAl_{1-x})_yGa_{1-y}N$層31がない場合に比べて50%以上の電子濃度の向上が図られる。このように、本発明の実施形態4によるFETによれば、電子を極薄いチャンネル層43に効率よく閉じ込めると同時に、チャンネルの電子濃度を大幅に向上できるので、高出力のGaN系FETが得られる。またゲート長を短縮した場合にFETのドレインコンダクタンスが大きく劣化しないので、高周波特性も向上させやすいという利点も有している。

【0035】GaNとその上に成長されたInAlN歪

層について、分極の効果によってどの程度の電荷がヘテロ界面に誘起されるかについて、ここで考察する。GaNは歪んでおらず、InAlNのみが歪んでいるものとする。ヘテロ界面で電束が分極の効果により変化を受けるが、これにはGaNとInAlNにおける自発分極の差と、InAlN膜に発生する歪によるピエゾ分極の寄与がある。F. Bernardini達によりPhysical Review vol. 56, pp. R10024-R10027(1997)の文献に報告されている理論値を用いるとAlN、GaN、InNの自発分極はそれぞれ$-0.081C/m^2$、$-0.029C/m^2$、$-0.032C/m^2$であるのでInN組成比がxの$In_xAl_{1-x}N$における自発分極は線形補間で近似すれば$Psp(x)=-0.081+0.049x$で求められる。従ってヘテロ界面での自発分極の変化は$Psp(x)-(-0.029)C/m^2$で与えられる。一方$In_xAl_{1-x}N$中のピエゾ分極はGaNとの格子定数差に基づく歪み$e_{xx}(x)$を用い、ウルツ鉱型結晶の対称性を考慮することにより$Ppe(x)=2e_{xx}(x)\{e_{31}(x)-e_{33}(x)C_{13}(x)/C_{33}(x)\}$で与えられる。$e_{31}(x)$及び$e_{33}(x)$は$In_xAl_{1-x}N$の圧電定数、$C_{13}(x)$及び$C_{33}(x)$は$In_xAl_{1-x}N$の弾性定数であり、以上のパラメータは報告されている理論値をもとに線形補間を用いて以下のように求められる。

$e_{31}(x)=-0.6+0.03x\ C/m^2$、$e_{33}(x)=1.46-0.49x\ C/m^2$、$C_{13}(x)=108-16x\ Gpa$、$C_{33}(x)=1.46-0.49x\ Gpa$、$e_{xx}(x)=(3.189-a(x))/a(x)$、$a(x)=3.112+0.428x$

これらの値をもちいて、ヘテロ界面の電荷を計算した結果を図7aに示す。この図から$In_xAl_{1-x}N$のInN組成比が0.3付近では、分極の変化が$In_xAl_{1-x}N$とその下のGaNとの間で殆ど無く、ヘテロ界面に発生する分極に起因した電荷量は0に近い。一方、InN組成比が0.4の場合はヘテロ界面におよそ$1.5\times10^{13}\times q/cm^2$の負の電荷が発生する。ここでqは電子1個の電荷である。このことから層構造が逆の場合、すなわち$In_xAl_{1-x}N$歪み層の上に形成されたGaNチャンネル層を想定するとヘテロ界面には分極の効果によって正の電荷が発生し、これによってヘテロ界面のポテンシャルの低い側GaNチャンネル層側に電子が$1.5\times10^{13}/cm^2$程度蓄積されることとなる。以上の考察から、$In_xAl_{1-x}N$のInN組成比は0.3以上であればよいことがわかる。しかしながら電子がチャンネル層に蓄積することが必要であるので$In_xAl_{1-x}N$のInN組成比の上限は$In_xAl_{1-x}N$のエネルギーバンドギャップがGaNの値よりも少なくとも大きい必要があることから決定され、その値はおよそ0.7となる。

【0036】$(In_xAl_{1-x})_yGa_{1-y}N$層31のxおよびyの設定については、上記考察に基づき次のように決定される。図7bは$(In_xAl_{1-x})_yGa_{1-y}N$系材料の格子定数とエネルギーギャップを示している。直線aはGaNに対応する点と$In_{0.3}Al_{0.7}N$に対応する点を結んだものであり、理論的にこの直線上の組成の材料をGaN上に形成すると分極の差が殆ど現れない。直線bはGaNに対応する点と$In_{0.4}Al_{0.6}N$に対応する点を結んだものであり、この直線上の組成の材料にGaNを形成すると分極の差異によって$1.5\times10^{13}/cm^2$程度の電子濃度がヘテロ界面に蓄積する。直線cはGaNに対応する点と$In_{0.7}Al_{0.3}N$に対応する点を結んだものであり、xの上限を示すものである。領域AはGaNと格子不整は起こすものの、電子デバイスに十分使用可能な領域で、格子定数として0.314nmから0.323nmの範囲である。従って三角形PQRで示された領域が本発明で使用可能であるが、チャンネル層にGaNを使用する場合はある程度の伝導体の不連続値が要求されるので、三角形SQTの内部の領域を用いる必要がある。いずれにせよ、$(In_xAl_{1-x})_yGa_{1-y}N$層31におけるxの値の範囲は0.3〜0.7である。一方yの値はチャンネル層43にGaNを用いる場合、およそ0.15〜0.6の範囲、チャンネル層43にInGaN層を用いる場合は0〜0.6の範囲が適切であり、共にxの値に応じて格子定数が0.323nm以下となる領域を用いることが望ましい。

【0037】(実施の形態5)実施形態4では表面がIII族原子面の場合について述べたが、表面がV族原子面となる成長条件で結晶成長を行う場合には、分極の方向が反対向きになるので、実施形態4での層構造の順序が逆になる。すなわち、図5におけるAlGaN層5の部分が$(In_xAl_{1-x})_yGa_{1-y}N$層に、図5の$(In_xAl_{1-x})_yGa_{1-y}N$層31がAlGaN層となり、他は変化がない。xやyの値も実施形態4で述べた領域を用いればよい。この構造を用いることの利点は実施形態4で述べたこととおなじである。

【0038】なお、本発明における面内で引っ張り応力を受けるAlGaN層5は面内で引っ張り応力をうけるかぎりこの層にInを加えてもよい。すなわちInAlGaNの4元混晶を用いてもよいことは言うまでもない。

【0039】以上の説明では、電解効果トランジスタを例にして説明したが、本発明は電解効果トランジスタには限定されない。本発明は、$(In_xAl_{1-x})_yGa_{1-y}N$($0\leqq X\leqq1$、$0\leqq Y\leqq1$)で表される窒化ガリウム系半導体のヘテロ構造を有する半導体装置に適用され得る。

【0040】なお、本発明で示したGaNバッファー層2は基板1上に層厚が100nm程度の比較的薄いAlN層を介して形成される場合が従来より報告されている

が、本発明はそのような場合にも本質的に何ら変わることなく適用できることは言うまでも無い。

【0041】

【発明の効果】上記で説明したように、本発明の半導体装置のある実施形態では、GaNバッファー層中に低AlN組成のAlGaN分離層を導入することにより、GaN層中の意図せず導入される残留キャリアに起因するソース・ドレイン間リーク電流、ゲートリーク電流、素子間リーク電流を著しく改善すると同時に、電子のチャンネル層への閉じ込めを効果的に行い、短ゲート長のデバイス特性を改善することに貢献する。また本発明の半導体装置の別の実施形態は、ひとつのチャンネル層に電子を蓄積できる新たな構造によって、高い相互コンダクタンスと高い電流駆動能力を有するダブルドープ型のGaN系ヘテロ構造FETを提供するものであり、窒化ガリウム系半導体素子のパワー特性向上や短ゲート長のデバイス特性を改善することに貢献するものである。

【図面の簡単な説明】

【図1a】本発明の実施形態1による半導体装置であるFETの断面図である。

【図1b】図1aに示される本発明のFETの深さ方向のポテンシャル形状を説明するポテンシャル図である。

【図2】本発明の実施形態1によるFETのシート電子濃度の温度特性を示す図である。

【図3a】従来のヘテロ構造FETのドレイン電圧ー電流特性を示す図である。

【図3b】本発明の実施形態1に関わるFETの、ドレイン電圧ー電流特性を示す図である。

【図4】本発明の実施形態3による半導体装置であるFETの断面図である。

【図5】本発明の実施形態4による半導体装置であるFETの断面図である

【図6】本発明の実施形態4によるFETにおける深さ方向のポテンシャル形状の説明するポテンシャル図である。

【図7a】本発明の実施形態4によるFETに適したInAlGaNの混晶の組織比領域について説明するためのInAlNにおける組成比と分極により発生するInAlNとGaNのヘテロ界面における電荷量の関係を示す図である。

【図7b】本発明の実施形態4によるFETに適したInAlGaNの混晶の組成比領域について説明するための、エネルギーギャップと格子定数の関係を示す図である。

【図8】従来のGaN系電界効果トランジスタの断面図である

【図9】従来のダブルドープダブルヘテロ構造における深さ方向のポテンシャルエネルギー形状の説明するポテンシャル図である。

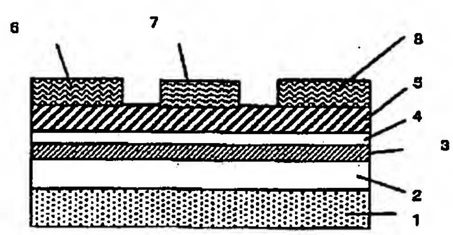
【図10】従来のGaN系ダブルドープダブルヘテロ構造の電界効果トランジスタの断面図である。

【図11】従来のGaN系ダブルドープダブルヘテロ構造における深さ方向のポテンシャルエネルギー形状の説明するポテンシャル図である。

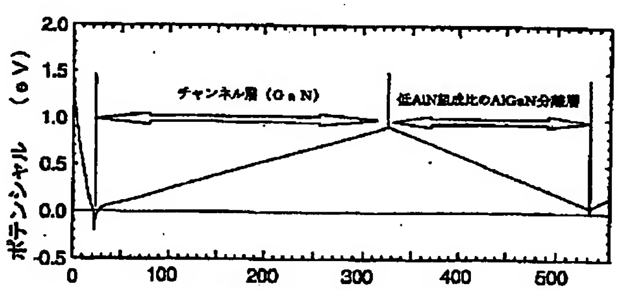
【符号の説明】

1	サファイアまたはSiC基板
2	GaNバッファー層
3	低AlN組成比のAlGaN分離層
4	チャンネル層
5	AlGaN層
6	ソース電極
7	ゲート電極
8	ドレイン電極
13	AlGaN層
31	InAlGaN層
41	GaN層
42	InGaN層
43	チャンネル層

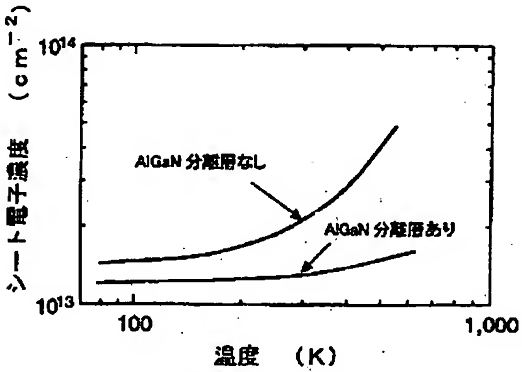
【図1a】



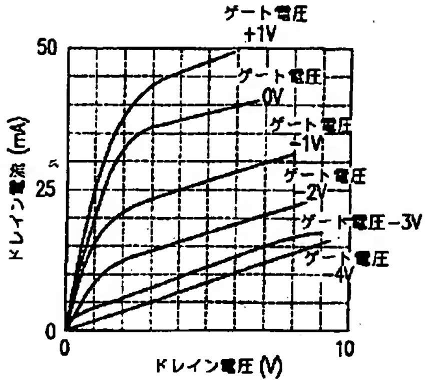
【図1b】



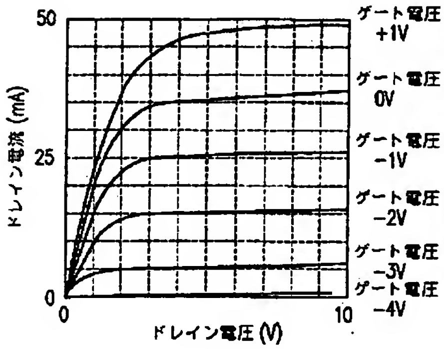
【図2】



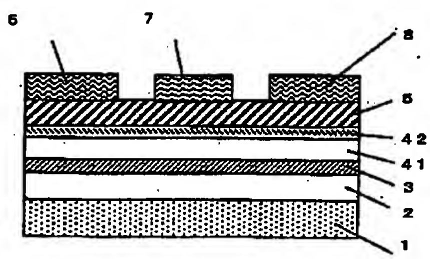
【図3a】



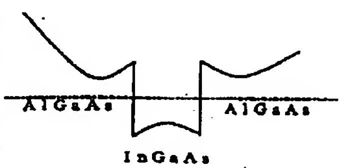
【図3b】



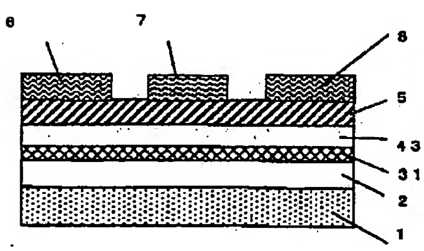
【図4】



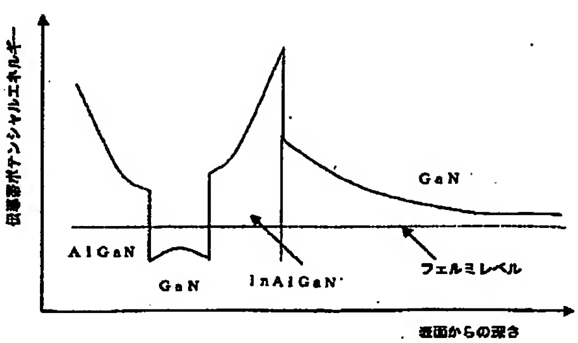
【図9】



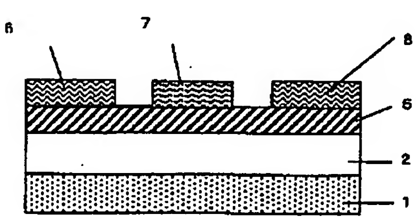
【図5】



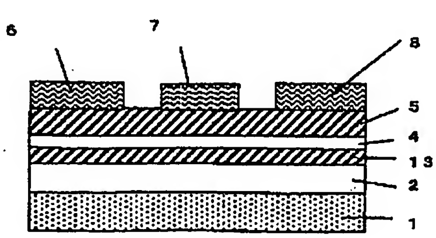
【図6】



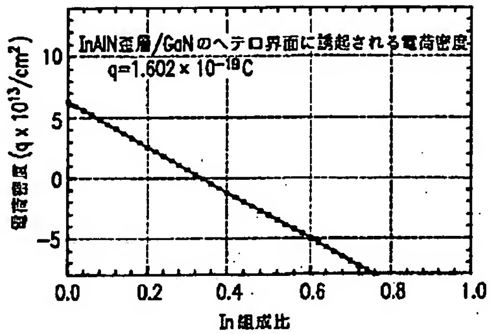
【図8】



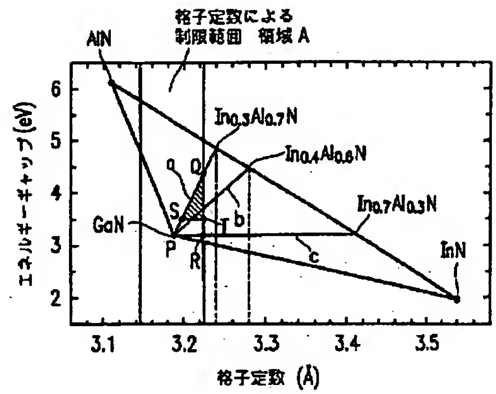
【図10】



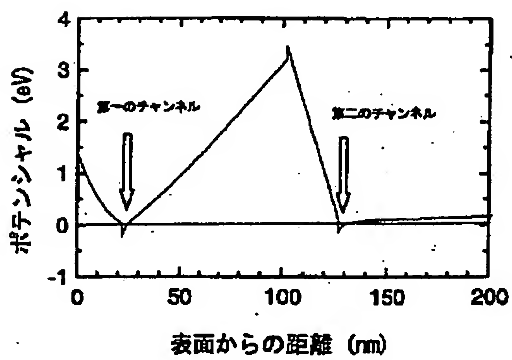
【図7a】



【図7b】



【図11】



フロントページの続き

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Fターム(参考)　5F102 FA00 GB01 GC01 GD01 GJ02 GJ10 GK04 GL04 GM04 GQ01 GQ03 HC01

Description

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor device, and more particularly to a semiconductor device such as a field-effect transistor (FET) having a heterostructure of gallium nitride-based semiconductor which is generally represented as (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1).

[0003] 2. Description of the Related Art

[0004] A gallium nitride-based semiconductor such as GaN, AlGaN, InGaN, InAlGaN or the like has a high dielectric breakdown field, high thermal conductivity and a high electron saturation velocity, and thus is promising as a material for a high-frequency power device. Particularly in a semiconductor device having an AlGaN/GaN heterojunction structure, electrons accumulate with high density in the close vicinity of a heterojunction interface between AlGaN and GaN, and a so-called two-dimensional electron gas is formed. This two-dimensional electron gas exists in a spatially separated state from donor impurities added to AlGaN, and thus shows high electron mobility. A field-effect transistor having such a heterostructure is produced so that a source resistance can be reduced. Moreover, a distance d from a gate electrode to the two-dimensional electron gas is typically as short as tens of nanometers, and thus, even if a gate length Lg is as short as about 100 nm, the ratio of the gate length Lg to the distance d (i.e., aspect ratio) Lg/d, can be increased from 5 to about 10. Accordingly, semiconductor devices having an AlGaN/GaN heterostructure have a superior feature in that a field-effect transistor which has an insignificant short-channel effect and satisfactory saturation property can be readily produced. Moreover, a two-dimensional electron of the AlGaN/GaN-based heterostructure has an electron velocity in a high field region of about 1*10V/cm, which is twice or more than the electron velocity in AlGaAs/InGaAs-based heterostructure currently prevalent as a high-frequency transistor, and thus, is expected to be applied to high-frequency power devices.

[0005] FIG. 8 shows an exemplary cross-sectional view of a conventional FET 800 having an AlGaN/GaN-based heterostructure. The AlGaN/GaN-based heterostructure of the FET 800 is typically formed on a substrate 801 composed of a [0001] facet (c facet), through a crystal growth process using a metal-organic chemical vapor deposition method or a molecular beam epitaxy method. Typically, a sapphire substrate or SiC substrate is used as the substrate 801. In the FET 800, a buffer layer 802 including GaN and an electron supply layer 805 including AlGaN are sequentially provided on the sapphire or SiC substrate 801. On the electron supply layer 805, a source electrode 806, a gate electrode 807, and a drain electrode 808 are provided separately from one another. In the case of forming the buffer layer 802 including GaN on the sapphire or SiC substrate 801, it is necessary to thickly form the buffer layer 802 in order to account for a great lattice constant difference between the substrate 801 and the buffer layer 802. This is because the strain due to a lattice mismatch between the buffer layer 802 and the substrate 801 is sufficiently relaxed by forming the buffer layer 802 so as to have a relatively large thickness. By forming the electron supply layer 805 containing AlGaN to which n-type impurities, such as Si or the like, are added so as to have a thickness on the order of tens of nanometers on the thick buffer layer 802, a two-dimensional electron gas (i.e., electron channel) is formed in the buffer layer 802 which has a great electron affinity in the heterointerface between the buffer layer 802 and the electron supply layer 805 (i.e., between AlGaN and GaN) due to the effects of selective doping. The crystal facet of a heterostructure formed by an MOCVD (Metal-Organic Chemical Vapor Deposition) method, is typically composed of a facet of Ga, which is a group III element. This two-dimensional electron gas is susceptible to the effects of piezo-polarization in a c axis direction due to tensile stress imposed on AlGaN, in addition to a difference in spontaneous polarization between AlGaN (included in the electron supply layer 805) and GaN (included in the buffer layer 802). Thus, electrons accumulate at a density which is higher than a value which would be expected from the density of the n-type impurities added to the electron supply layer 805. When the Al composition of AlGaN of the electron supply layer 805 is 0.2 to 0.3 with respect to AlGaN, electron density of the channel layer formed in the buffer layer 802 is about 1*10/cm, which is about 3 times the density of a GaAs-based device. Since the two-dimensional electron gas at such a high density is accumulated, the semiconductor device 800 used as a GaN-based heterostructure field-effect transistor (FET) is considered as a highly promising power device.

[0006] However, such a conventional FET 800 has several disadvantages. The first of which is that due to the immaturity of crystal growth techniques, a crystal with satisfactory quality cannot be obtained.

[0007] One of the problems related to the crystal growth is associated with the fact that the undoped GaN included in the buffer layer 802 typically is an n-type and the carrier density may be as high as about 10/cmor more. This is presumably because constituent nitrogen (N) atoms are released during crystal growth, and thus, vacancies are liable to be formed. When there are such residual carriers, the leakage current component via the buffer layer 802 of the device becomes greater. In particular, when operating the device at a high temperature, deteriorations in the element properties, such as aggravation of pinch-off characteristics, may occur. As for an isolation problem, when forming a plurality of GaN-based heterostructure FETs on the same substrate, the FETs interfere with each other, hindering normal operation. When the gate electrode 807 is further provided above this buffer layer 802, a problem such as an increase of a gate leakage current, or the like, may arise.

[0008] The second disadvantage of a conventional FET 800 is ascribed to the effects of polarization as described above. In a conventional FET having an AlGaAs/InGaAs-based heterostructure, a channel layer is composed of InGaAs, and an electron (carrier) supply layer is composed of AlGaAs and is doped with Si. In general, when such a FET is applied as a power device, an AlGaAs/InGaAs/AlGaAs structure, in which an InGaAs (channel) layer is sandwiched by two n-type AlGaAs layers, is employed. In this structure, the electron density of the channel layer is about 2 times the electron density of a channel layer in a non-sandwich type structure. FIG. 9 schematically shows a distribution of the potential energy of conduction band along the depth direction of such a semiconductor device. As shown in FIG. 9, electrons are supplied from the AlGaAs layers to the InGaAs layer whose potential is lower than those of the AlGaAs layers. Such a structure

which has two Si-doped AlGaAs layers is called a double-doped structure or a double-doped, double-heterostructure.
[0009] FIG. 10 shows a structure of an n-type AlGaN/GaN/n-type AlGaN device 1000, which is a GaN-based device having a double-doped structure. FIG. 11 shows a distribution of the potential energy along the depth direction in the semiconductor device 1000.
[0010] The conventional FET 1000 shown in FIG. 10 sequentially includes the following layers on a sapphire or SiC substrate 1001: a first channel layer 1002, including GaN; a first electron supply layer 1013, including AlGaN; a second channel layer 1004, including GaN; and a second electron supply layer 1005, including AlGaN. On the second electron supply layer 1005, a source electrode 1006, a gate electrode 1007 and a drain electrode 1008 are provided separately from one another. In the GaN-based double-doped structure shown in FIG. 10, doping is performed only on the second electron supply layer 1005 because a large polarization influence is caused on electrons which are supplied from the first and second electron supply layers 1013 and 1005 to the first and second channel layers 1002 and 1004, respectively.
[0011] As seen from the graph of FIG. 11, in a GaN-based semiconductor device, the potential in a heterointerface between the second channel layer 1004 and the first electron supply layer 1013 is significantly increased due to piezo-polarization or spontaneous polarization. As a result, electrons accumulate in two separate regions. That is, a first (lower) electron channel is formed by electrons which have accumulated in the first channel layer 1002 in the close vicinity of a heterointerface with the first electron supply layer 1013, and a second (upper) electron channel is formed by electrons which have accumulated in the second channel layer 1004 in the close vicinity of a heterointerface with the second electron supply layer 1005. Currents flow through these electron channels. The distance between the first and second electron channels is about several tens of nanometers. With such a great distance, the mutual conductance of the conventional FET 1000 is small as compared with an AlGaAs/InGaAs/AlGaAs structure in which electrons accumulate so as to form a single electron channel. As a result, the gain of the conventional FET 1000 is decreased, which is undesirable in view of high frequency operation.

SUMMARY OF THE INVENTION
[0012] According to one aspect of the present invention, a semiconductor device includes: a substrate; a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of Ga atoms; a separating layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the buffer layer, wherein surfaces of the separating layer are c facets of In, Al, or Ga atoms; a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the separating layer, wherein surfaces of the channel layer are c facets of Ga or In atoms; and an electron supply layer including AlGaN formed on the channel layer, wherein surfaces of the electron supply layer are c facets of Al or Ga atoms, wherein the AlN composition ratio in the separating layer is smaller than the AlN composition ratio in the electron supply layer.
[0013] In one embodiment of the present invention, in the separating layer including (InXAl1-X)YGa1-YN, X=0.
[0014] In another embodiment of the present invention, the AlN composition ratio in the separating layer is equal to or smaller than about 0.1.
[0015] Instill another embodiment of the present invention, the AlN composition ratio in the separating layer gradually increases from an interface with the buffer layer to an interface with the electron supply layer.
[0016] According to another aspect of the present invention, a semiconductor device includes: a substrate; a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of Ga atoms; a first electron supply layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the buffer layer, wherein surfaces of the first electron supply layer are c facets of In, Al, or Ga atoms; a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the first electron supply layer, wherein surfaces of the channel layer are c facets of Ga or In atoms; and a second electron supply layer including AlGaN formed on the channel layer, wherein surfaces of the electron supply layer are c facets of Al or Ga atoms, wherein the AlN composition ratio, the InN composition ratio, and the GaN composition ratio in the first electron supply layer are set such that electrons accumulate in a vicinity of a heterointerface between the first electron supply layer and the channel layer due to a variation in polarization.
[0017] According to still another aspect of the present invention, a semiconductor device includes: a substrate; a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of N atoms; a first electron supply layer including AlGaN formed on the buffer layer, wherein surfaces of the first electron supply layer are c facets of N atoms; a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the first electron supply layer, wherein surfaces of the channel layer are c facets of N atoms; and a second electron supply layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the channel layer, wherein surfaces of the electron supply layer are c facets of N atoms, wherein the AlN composition ratio, the InN composition ratio, and the GaN composition ratio in the first electron supply layer are set such that electrons accumulate in a vicinity of a heterointerface between the second electron supply layer and the channel layer due to a variation in polarization.
[0018] Thus, the invention described herein makes possible the advantages of: (1) providing a semiconductor device in which a leakage current between a source and a drain, a gate leakage current, and a leakage current between devices caused by residual carriers caused in a GaN layer (channel layer) are significantly reduced; and (2) providing a semiconductor device having a double-doped, GaN-based heterostructure in which electrons can accumulate so as to form a single electron channel and which provides a superior mutual conductance and a high current driving performance.
[0019] These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS
[0020] FIG. 1A is a cross-sectional view of a field-effect transistor (FET) which is a semiconductor device according to embodiment 1 of the present invention.
[0021] FIG. 1B is a potential map showing a distribution of potential energy along a depth direction of the FET shown in FIG. 1A.
[0022] FIG. 2 shows a temperature characteristic of the sheet electron density for the FET according to embodiment 1 of the present invention and for a conventional FET.
[0023] FIG. 3A shows a drain voltage-current characteristic of a conventional heterostructure FET.
[0024] FIG. 3B shows a drain voltage-current characteristic of the FET according to embodiment 1 of the present invention.
[0025] FIG. 4 is a cross-sectional view of a FET which is a semiconductor device according to embodiment 3 of the present invention.
[0026] FIG. 5 is a cross-sectional view of a FET which is a semiconductor device according to embodiment 4 of the present invention.
[0027] FIG. 6 is a potential map showing a distribution of a potential energy along a depth direction in the FET shown in FIG. 5.
[0028] FIG. 7A shows the relationship between an In composition ratio in InAlN and a charge density in a heterostructure between InAlN and GaN.
[0029] FIG. 7B is a graph showing the relationship between a lattice constant and an energy gap for describing a composition ratio of an InAlGaN mixed crystal which is suitable for a FET according to embodiment 4 of the present invention.
[0030] FIG. 8 is a cross-sectional view of a conventional GaN-based FET.
[0031] FIG. 9 is a potential map showing a distribution of potential energy along a depth direction of a conventional double-doped, double heterostructure.
[0032] FIG. 10 is a cross-sectional view of a conventional GaN-based double-doped, double heterostructure.
[0033] FIG. 11 is a potential map showing a distribution of potential energy along a depth direction of the conventional GaN-based double-doped, double heterostructure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS
[0034] In the description hereinbelow, a field-effect transistor (FET) is taken as an example of the present invention. However, the present invention is not limited to a field-effect transistor. The present invention can be applied to any semiconductor device having a heterostructure of a gallium nitride-based semiconductor which is generally represented as (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1).
[0035] As described above with reference to FIG. 10, in a structure including the first channel layer 1002, the first electron supply layer 1013, the second channel layer 1004, and the second electron supply layer 1005, two separated electron channels are formed. In such a structure, a large number of electrons accumulate in both of these two regions, but electrons in the lower electron channel do not largely contribute to an increase in drain current. These electrons increase the gate capacitance of the FET, but deteriorate the performance of the FET as a whole. However, in such a structure, increase in potential level at the heterointerface between the first electron supply layer 1013 composed of AlGaN and the second channel layer 1004 composed of GaN contributes to the confinement of electrons originally present in the upper portion of the semiconductor device into an upper (second) electron channel. With such an electron confinement effect, the drain conductance of the FET is decreased, whereby the power gain of the FET is increased. Furthermore, in such a FET, the gate length can be easily decreased, and accordingly, the operation frequency can be increased.
[0036] A semiconductor device according to one embodiment of the present invention has substantially the same structure as that shown in FIG. 10, except that a layer corresponding to the second electron supply layer 1005 shown in FIG. 10 (hereinafter, referred to as a "separating layer") is formed so as to have a thickness greater than that of the second electron supply layer 1005, and that the AlN composition ratio in the separating layer is set to be much smaller than the AlN composition ratio in an electron supply layer (corresponding to the first electron supply layer 1013). In the semiconductor device having such a structure, electrons are prevented from accumulating in the close vicinity of a heterointerface between the separating layer and a buffer layer (corresponding to the second channel layer 1004), while the increase in potential level at the heterointerface contributes to the confinement of electrons.
[0037] In a semiconductor device according to another embodiment of the present invention, a first electron supply layer is not composed of AlGaN, but of (InXAl1-X)YGa1-YN With such a material, at the heterointerface between the first electron supply layer and the buffer layer, the sign (+/-) of the peak potential level is opposite to that seen in the case where AlGaN is used for the separating layer. In such a semiconductor device, an electron channel is formed only in the channel layer, while an electron channel is not formed in the buffer layer. As a result, a potential distribution similar to that seen in a selectively-doped, AlGaAs/InGaAs/AlGaAs double heterostructure can be obtained. That is, by setting X and Y in (InXAl1-X)YGa1-YN to appropriate values, electrons in the first electron supply layer can be supplied to the electron channel in the channel layer. In the case where such a structure is employed, for the purpose of substantially obtaining a single electron channel, it is necessary to set the thickness of the channel layer (which is formed of GaN, InGaN, or a combination of GaN and InGaN over the (InXAl1-X)YGa1-YN layer) from about 10 nm to about 20 nm.
[0038] (Embodiment 1)
[0039] A semiconductor device according to embodiment 1 of the present invention is described with reference to the

drawings. FIG. 1A is a cross-sectional view of a FET 100 according to embodiment 1 of the present invention. FIG. 1B shows a distribution of potential energy along a depth direction of the FET 100 when the gate voltage is 0 V.

[0040] The FET 100 includes on a substrate 101 a buffer layer 102, a separating layer 103, a channel layer 104, and an electron supply layer 105. On the electron supply layer 105, a source electrode 106, a gate electrode 107, and a drain electrode 108 are provided separately from one another.

[0041] The FET 100 is formed, for example, as described below. On a sapphire substrate 101, a GaN layer (thickness: about 20 nm) and an undoped GaN layer (thickness: about 2 [mu]m) are sequentially grown by using a MOCVD method. These GaN layers form a buffer layer 102. Then, on the buffer layer 102, an AlGaN separating layer 103 (thickness: about 50 nm to about 300 nm) is formed such that the composition ratio of AlN with respect to AlGaN in the separating layer 103 is about 0.1 or less (and is of course greater than 0), preferably from about 0.01 to about 0.05. On the separating layer 103, a GaN channel layer 104 (thickness: about 300 nm to about 500 nm) is formed. On the channel layer 104, an n-type AlGaN electron supply layer 105 doped with Si (thickness: about 20 nm) is formed, in which the carrier density is, for example, about 2*10cm. The surfaces (interfaces) of these layers are composed of a group III element.

[0042] FIG. 1B shows a potential profile of a semiconductor device having the structure shown inFIG. 1A, in which the separating layer 103 has a thickness of about 200 nm and has an AlN composition ratio of 0.01; the channel layer 104 has a thickness of about 300 nm; and the electron supply layer 105 has a thickness of about 20 nm. In this case, a depletion layer which is formed by the separating layer 103 and the channel layer 104 has a thickness of about 500 nm, and the peak value of the potential is 1 eV as seen from FIG. 1B. The potential at a heterointerface on the substrate side (i.e., the interface between the separating layer 103 and the buffer layer 102) is higher than the Fermi level (at which the potential is 0 eV). The electron density at this heterointerface is sufficiently low, e.g., on the order of 10/cm. Furthermore, the heterointerface at the substrate side is completely separated from the heterointerface at the upper side (closer to the upper surface of the FET 100) by the thick depletion layer.

[0043] Such a FET structure is different from the structure of the conventional FET 800 (FIG. 8) in that the above FET structure includes an AlGaN separating layer 103 whose AlN composition ratio is low. With this separating layer 103, the carrier density and its temperature dependency significantly improve.

[0044] FIG. 2 shows the variation of sheet electron density with temperature for the FET 800 which has a conventional heterostructure including a GaN buffer layer, and for the FET 100 in which an AlGaN separating layer 103 with a low AlN composition ratio is provided over the buffer layer 102. The sheet electron density in the FET 100 was measured by a hole measurement method. As seen from FIG. 2, in the FET 100 according to embodiment 1 of the present invention, the electron density is substantially constant in a range from about 77 K to room temperature, although it slightly increases in a higher temperature range. It is recognized that this constant electron density corresponds to the density of a two-dimensional electron gas accumulated in the close vicinity of a heterointerface between the electron supply layer 105 and the channel layer 104. On the other hand, in the conventional FET 800 which does not have an AlGaN separating layer 103 with a low AlN composition ratio, the electron density is high, and its temperature dependency is large. In the FET 800, it is recognized that the increase in electron density along with the increase in temperature is ascribed to the ionization of donors in the GaN buffer layer 802. In the FET 800 not having the AlGaN separating layer 103 with a low AlN composition ratio, the measured electron density is the electron density in the entire buffer layer 802, whereas in the structure of the FET 100, the influence of an ohmic electrode is blocked by the AlGaN separating layer 103 with a low AlN composition ratio (which is a depletion layer having a high resistance), whereby the generation of ions in the buffer layer 102 is suppressed. Therefore, the measured electron density does not include the electron density in the buffer layer 102 under the separating layer 103.

[0045] FIGS. 3A and 3B show typical static characteristics of the conventional FET 800 and the FET 100 according to embodiment 1 of the present invention, respectively. As seen from FIG. 3B, the FET 100 has satisfactory pinch-off characteristics, so that drain current is not generated at a gate voltage of about -4 V. On the other hand, in the FET 800, as seen from FIG. 3A, the drain current is not blocked, and this current flows as a leakage current. In the case where an integrated circuit is formed on a single board by a plurality of such devices, each of which generating a large leakage current, adjacent devices interfere with one another, resulting in abnormal operation. Furthermore, the amount of ineffective current components increases, whereby the efficiency of the power device and high frequency operation are deteriorated.

[0046] As described above, the FET 100 according to embodiment 1 of the present invention includes between the buffer layer 102 and the channel layer 104 the separating layer 103 composed of AlGaN having a low AlN composition ratio. In such a structure, increase in a leakage current between a source and a drain, increase in a gate leakage current, and increase in current leakage between devices, due to residual carriers which may be caused in the buffer layer 102, are effectively suppressed. As a result, the suppressed increase of leakage currents contribute to the improvement in characteristics of a high frequency power device and to the prevention of abnormal operation in an integrated circuit made of a high frequency power device(s).

[0047] Now, the details of the separating layer 103 are described. Some conventional devices includes a thin film of AlGaN like the separating layer 103, but the function thereof is different from that of the separating layer 103. The exemplary conventional semiconductor device shown in FIG. 10 also includes an AlGaN thin film, but the AlN composition ratio and the location thereof in the layered structure are completely different from those of the separating layer 103 in the FET 100 of the present invention.

[0048] R. Gaska, et al., "Two-channel AlGaN/GaN heterostructure field effect transistor for high power applications" (Journal of Applied Physics vol. 85 (1999) pp. 3009-3011) describes a double-channel heterostructure FET having a structure similar to that of the FET according to the present invention. This FET includes a sapphire substrate and

the following layers sequentially provided thereon: a first AlGaN layer (thickness: 50 nm); a GaN layer (thickness: 800 nm); a second AlGaN layer (thickness: 25 nm); a GaN channel layer (thickness: 100 nm); and an AlGaN barrier layer (thickness: 30 nm). The second AlGaN layer in this layered structure may appear to correspond to the AlGaN separating layer and to have the same function as that of the AlGaN separating layer of the present invention. However, as the title of the paper states, Gaska et al's purpose is to make two electron channels in the FET, and for this purpose, the GaN channel layer is formed so as to be as thin as 100 nm. Accordingly, the distance between the upper surface of the FET and the lower electron channel is as short as 150 nm. Furthermore, in this FET, the AlGaN composition ratio in the second AlGaN layer is the same as that in the AlGaN barrier layer, and therefore, this second AlGaN layer cannot be made thick. This is because the thickness of the second AlGaN layer is limited by its critical thickness which is imposed due to a lattice mismatch with the GaN channel layer, and also because if the second AlGaN layer is thick, the potential excessively increases in a heterointerface between the second AlGaN layer and the GaN channel layer, and accordingly, holes accumulate in this heterointerface. In the case where the hole density becomes relatively high, the variation of hole density (which depends on the variation of gate voltage) increases, and accordingly, the gate capacitance which depends on the hole density may be increased to a non-negligible level. As a result, the high frequency characteristic of the FET is deteriorated. In order to improve the high frequency characteristic, it is important to prevent the accumulation of holes or to provide a sufficient distance between the upper surface of the FET and a region in which holes accumulate so that the variation of electric charge caused by the variation of gate voltage or drain voltage is decreased as much as possible.
[0049] The first feature of the FET according to embodiment 1 of the present invention is that the AlN composition ratio of the AlGaN separating layer 103 is sufficiently lower than that of the AlGaN electron supply layer 105, so that electrons are prevented from accumulating in the close vicinity of a heterointerface between the separating layer 103 and the buffer layer 102. The second feature of the FET according to embodiment 1 of the present invention is that the thickness of the separating layer 103 is large, whereby a desirable potential level is obtained in the heterointerface. The third feature of the FET according to embodiment 1 of the present invention is that the sufficient distance is provided between the upper surface of the FET and the separating layer 103, so that only a single electron channel is formed in the FET. In such a structure, it is important to appropriately determine the thickness of the channel layer 104 (i.e., to make sure that the thickness of the channel layer 104 is not much greater than the appropriate thickness).
[0050] Now, an appropriate thickness of the channel layer 104 is approximately estimated. The tolerance of an excessive carrier density which is defined by the density of donors unintentionally caused in the channel layer 104 is considered to be a about {fraction (1/50)} to about {fraction (1/100)} or less of the saturated two-dimensional electron gas density. In such a case, the sheet carrier density is about 1*10/cmto about 3*10/cm. Assuming that the residual donor density is about 1*10/cm, and setting the peak potential to about 2 eV in view of the GaN bandgap of about 3.2 eV, the thickness of the depleted GaN channel layer 104 is about 460 nm. Assuming that the residual donor density is about 5*10/cm, the thickness of the GaN channel layer 104 is about 205 nm. Taking account of the typical thickness of the channel layer (about 50 nm to about 100 nm), it is recognized that an appropriate thickness of the channel layer 104 is about 250 nm to about 560 nm.
[0051] In view of the above, the appropriate thickness of the GaN channel layer 104 is estimated to be about 300 nm to about 500 nm. This thickness is sufficiently greater than a typical depth to which an electrode metal material is inserted from the upper surface of the FET under the conditions for forming a common ohmic electrode (i.e., about 100 nm or less). In addition, since the AlGaN separating layer 103 having a low AlN composition ratio is provided under the channel layer 104, no current flows through the buffer layer 102. Moreover, the density of a two-dimensional electron gas accumulated in the close vicinity of the heterointerface between the separating layer 103 and the GaN buffer layer 102 is low. Therefore, the gate capacitance does not significantly increase, and the high frequency characteristic of the FET is not deteriorated.
[0052] (Embodiment 2)
[0053] A FET according to embodiment 2 of the present invention has substantially the same structure as that of the FET according to embodiment 1, except that a separating layer 103 is formed such that the AlN composition ratio thereof gradually increases along the thickness direction from the lower surface to the upper surface. Specifically, the separating layer 103 is formed so as to have a thickness of, e.g., about 100 nm to about 300 nm such that the AlN composition ratio gradually increases from about 0 to about 0.05 in a growth direction, i.e., from the lower surface to the upper surface thereof. The change rate of the AlN composition ratio is not limited to a particular rate as long as it is positive, i.e., the AlN composition ratio increasingly upwardly changes in a growth direction. In this way, the difference in composition at the heterointerface between the separating layer 103 and the buffer layer 102 is decreased. As a result, the density of electrons which accumulate in the close vicinity of this heterointerface is decreased, whereby the gate capacitance can be decreased.
[0054] (Embodiment 3)
[0055] A FET 400 according to embodiment 3 of the present invention is described with reference to FIG. 4.
[0056] The FET 400 sequentially includes the following layers on a substrate 401: a buffer layer 402; a separating layer 403; a first sub-channel layer 441; a second sub-channel layer 442; and an electron supply layer 405. On the electron supply layer 405, a source electrode 406, a gate electrode 407, and a drain electrode 408 are provided separately from one another.
[0057] The FET 400 includes two layers, the first sub-channel layer 441 composed of GaN and the second sub-channel layer 442 composed of InGaN, in place of the channel layer 104 of the FET 100. The structure of the FET 400 is achieved by providing an additional layer between the channel layer 104 and the electron supply layer 105 as the second sub-channel layer 442. The energy bandgap in the second sub-channel layer 442 is set to be smaller than in the first sub-channel layer 441 (corresponding to the channel layer 104), so that the electrons density in the electron channel is

increased. As a result, electrons are confined in the second sub-channel layer 442, and accordingly, the gate length of the FET 400 can be easily decreased. The layered structure of the FET 400 is substantially the same as that of the FET 100, except for the inclusion of the InGaN second sub-channel layer 442. The InN composition ratio of the second sub-channel layer 442 with respect to InGaN is appropriately about 0.05 to about 0.2. The thickness of the second sub-channel layer 442 is appropriately about 10 nm to about 20 nm. The surfaces (interfaces) of these layers are composed of a group III element.

[0058] (Embodiment 4)

[0059] As described above with reference to FIG. 10, in a conventional structure in which a thin AlGaN layer 1013 is provided between the GaN layers 1002 and 1004, two electron channels are formed, and holes or electrons readily accumulate in the close vicinity of the heterointerface between the layers 1013 and 1004 and in the close vicinity of the heterointerface between the layers 1013 and 1002, respectively, due to the effects of spontaneous polarization and piezo-polarization. In addition, the two electron channels are widely separated by several tens of nanometers. As a result, pinch-off characteristics are not satisfactory, and the capacitance is additionally increased, whereby the high frequency characteristic is deteriorated. A FET according to embodiment 4 of the present invention includes a novel heterostructure for solving such problems, in which an (InXAl1-X)YGa1-YN first electron supply layer is employed in place of the AlGaN first electron supply layer 1013.

[0060] An semiconductor device according to embodiment 4 of the present invention is described with reference to FIG. 5. FIG. 5 is a cross-sectional view of a FET 500 according to embodiment 4 of the present invention.

[0061] The FET 500 sequentially includes the following layers on a substrate 501: a buffer layer 502; a first electron supply layer 531; a channel layer 543; and a second electron supply layer 505. On the second electron supply layer 505, a source electrode 506, a gate electrode 507, and a drain electrode 508 are provided separately from one another.

[0062] The FET 500 is fabricated, for example, as follows. In the first step, a GaN buffer layer 502 (thickness: about 2 [mu] m) is grown on a sapphire or SiC substrate 501 by using a MOCVD method. On the GaN buffer layer 502, a first electron supply layer 531 including (InXAl1-X)YGa1-YN (thickness: about 10 nm to 30 nm) is grown. The (InXAl1-X)YGa1-YN first electron supply layer 531 may be doped with n-type impurities such that the doping density is on the order of about 1*10/cmto about 5*10/cm. The thickness of the first electron supply layer 531 is formed to be as thin as the critical thickness defined by a compression strain which is mainly imposed on this first electron supply layer 531.

[0063] On the first electron supply layer 531, a channel layer 543 is formed. The channel layer 543 may be formed solely as a GaN layer, solely as an InGaN layer, or as a combination of a GaN layer and an InGaN layer. However, it is important that in suppressing the decrease in the mutual conductance of the FET, the channel layer 543 is formed so as to be as thin as about 10 nm to about 30 nm. In the case where an InGaN layer is employed as the channel layer 543, the thickness thereof is appropriately set from about 10 nm to about 20 nm, and the InN composition ratio is appropriately set from about 0.05 to about 0.2. On the channel layer 543, a second electron supply layer 505 including n-type AlGaN is formed. The thickness thereof is appropriately set from about 10 nm to about 30 nm, the AlN composition ratio is appropriately set from about 0.15 to about 0.5, and the density of n-type impurity is appropriately set from about 1*10/cmto about 5*10/cm. The surfaces (interfaces) of these layers are composed of a group III element.

[0064] FIG. 6 is a potential map showing a distribution of a potential energy along the depth direction in the above heterostructure of the FET 500 including a GaN layer as the channel layer 543. The FET 500 uses an (InXAl1-X)YGa1-YN material for the first electron supply layer 531, whereby electrons are supplied to the channel layer 543 from both the (InXAl1-X)YGa1-YN first electron supply layer 531 and the AlGaN second electron supply layer 505, and can be confined in the channel layer 543. As a result, a potential distribution similar to that obtained in the AlGaAs/InGaAs/AlGaAs structure shown in FIG. 9 is obtained. In this case, the electron density in the channel layer 543 is increased by about 50% or more as compared to a case where the (InXAl1-X)YGa1-YN first electron supply layer 531 is not provided.

[0065] Thus, in the FET 500 according to embodiment 4 of the present invention, electrons are efficiently confined in the thin channel layer 543, while the electron density of the electron channel formed in the channel layer 543 can be significantly increased. As a result, a high-power GaN-based FET can be obtained. Moreover, since the drain conductance of the FET does not significantly deteriorate when the gate length is shortened, the high frequency characteristics can be readily improved.

[0066] Now, a consideration is given to how much electric charge is caused by the effects of polarization in a heterointerface between the GaN buffer layer 502 and an InAlN strain layer (an example of the first electron supply layer 531) formed thereon. Herein, it is assumed that no strain is caused in the GaN buffer layer 502, but a strain is caused only in the InAlN strain layer. In the heterointerface, an electric flux is subjected to the effects of polarization. The effects of polarization includes the effects resulting from difference of spontaneous polarization between the GaN buffer layer 502 and the InAlN strain layer, and the effects of piezo-polarization due to a strain caused in the InAlN strain layer. In the case of employing the theoretical values for the spontaneous polarizations of AlN, GaN, and InN, which are -0.081 C/m, -0.029 C/m, -0.032 C/m, respectively, (which are described in a document authored by F. Bernardini et al., in Physical Reviewvol. 56, pp. R10024-R10027 (1997)), the spontaneous polarization in InXAl1-XN (where X represents the InN composition ratio) is approximated using a linear interpolation method with the following expression:

Psp(x)=-0.081+0.049x.

[0067] Therefore, the variation of spontaneous polarization in the heterointerface is:

Psp(x)-(-0.029)C/m.

[0068] On the other hand, the piezo-polarization in InXAl1-XN is obtained using a strain exx(x) due to the difference in lattice constant between InXAl1-XN and GaN in view of the symmetry of a wurtzite crystal by the following expression:

Ppe(x)=2exx(x){e31(x)-e33(x)C13(x)/C33(x)}

[0069] where e31(x) and e33(x) are piezoelectric constants for InXAl1-XN, and C13(x) and C33(x) are elastic constants for InXAl1-XN. These parameters are obtained as follows using a linear interpolation method with the theoretical values reported by F. Bernardini et al. and those given by A. F. Wright "Elastic properties of zinc-blende and wurzite AlN, GaN, and InN," Journal of Applied Physics vol. 82 pp. 2833-2839 (1997):

e31(x)=-0.6+0.03x C/m,
e33(x)=1.46-0.49x C/m,
C13(x)=108-16x Gpa,
C33(x)=1.46-0.49x Gpa,
exx(x)=(3.189-a(x))/a(x),
a(x)=3.112+0.428x.

[0070] The calculation result of the electric charge in the heterointerface with these values is shown in FIG. 7A. As seen from this graph, in the case where the InN composition ratio is about 0.3, the electric charge which may be caused in the heterointerface due to polarization is approximately zero, because substantially no change is caused in the polarization between InXAl1-XN (the first electron supply layer 531) and GaN (the buffer layer 502). On the other hand, in the case where the InN composition ratio is about 0.4, a value of about 1.5*10*g/cmof negative electric charge (where q is the electric charge of one electron) is generated in the heterointerface. Accordingly, in the case where the layered structure is inversed, i.e., a GaN channel layer is formed on an InXAl1-XN strain layer, a positive electric charge is generated in the heterointerface due to the effects of polarization. As a result, about 1.5*10/cmelectrons accumulate in the vicinity of the heterointerface in the GaN channel layer whose potential is lower than that of the InXAl1-XN strain layer. Thus, in view of the above, the InN composition ratio in the InXAl1-XN strain layer is only required to be about 0.3 or more. However, since electrons need to accumulate in the channel layer, and the energy bandgap of InXAl1-XN needs to be greater than that of GaN, the upper limit of the InN composition ratio in the InXAl1-XN strain layer is about 0.7.

[0071] Values for X and Y in the (InXAl1-X)YGa1-YN first electron supply layer 531 are determined as follows based on the above discussion. FIG. 7B shows a relationship between the lattice constant and the energy gap in an (InXAl1-X) YGa1-YN-based material. Line (a) connects point P corresponding to GaN and point E corresponding to In0.3Al0.7N. In theory, in the case where a layer is formed of a material corresponding to a point on line (a) on a GaN layer, there is little polarization caused therebetween. Line (b) connects point P corresponding to GaN and point F corresponding to In0.4Al0.6N. In theory, in the case where a layer is formed of a material corresponding to a point on line (b) on a GaN layer, about 1.5*10/cmelectrons accumulate in the vicinity of the heterointerface in the GaN layer due to the difference in potential which is caused by the effects of polarization. Line (c) connects point P corresponding to GaN and point G corresponding to In0.7Al0.3N, and represents the upper limit of X. A material corresponding to a point in Region A causes a lattice mismatch with GaN, but is sufficiently available for an electron device. The Region A ranges from about 3.14 to about 3.28 for the lattice constant. Thus, a material corresponding to a point in a triangular region designated by PQR can be used in a FET according to the present invention. However, in the case where a GaN material is used for the channel layer, it is necessary to provide a certain difference in the minimum energy of conduction-band between the channel layer and the first electron supply layer, and accordingly, a material corresponding to a point in a triangular region designated by SQT should be used in a FET according to the present invention. In either case, the range of X in the (InXAl1-X)YGa1-YN first electron supply layer 531 is from about 0.3 to about 0.7. On the other hand, the range of Y in the (InXAl1-X)YGa1-YN is appropriately about 0.15-0.6 when the channel layer 543 is made of GaN, and is appropriately about 0 to about 0.6 when the channel layer 543 is made of InGaN. In either case, it is preferable to select a material such that its lattice constant is about 0.323 nm or less according to the value of X.

[0072] (Embodiment 5)

[0073] In the semiconductor device according to embodiment 4, the crystal facet of each layer is composed of a group III element. In a semiconductor device according to embodiment 5, on the other hand, the crystal facet of each layer is composed of a group V element. When the crystal growth is performed under the condition that the crystal facet of each layer is composed of a group V element, the direction of polarization is opposite to that for the crystal facet of a group III element. Therefore, the layered structure should be the inverse of the layered structure in the semiconductor device according to embodiment 4, i.e., a layer corresponding to the second electron supply layer 505 (FIG. 5) is an (InXAl1-X) YGa1-YN layer, and a layer corresponding to the first electron supply layer 531 (FIG. 5) is an AlGaN layer. As for the other details, the semiconductor device according to embodiment 5 is substantially the same as the semiconductor device according to embodiment 4. Values for X and Y may be determined in the same manner as described for embodiment 4. Advantages obtained from the device structure according to embodiment 5 are the same as those of the device structure according to embodiment 4.

[0074] In the above embodiments of the present invention, In can be contained in the AlGaN layer as long as the AlGaN layer is subjected to a tensile stress. That is, needless to say, a four-element mixed crystal, such as (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1), may be used for this layer.

[0075] In the above embodiments of the present invention, an AlN layer having a relatively thin thickness, such as about 100 nm, may be formed between the substrate and the buffer layer as in a conventional semiconductor device. Even in a case where such an AlN layer is formed, a semiconductor device according to the present invention can be used in essentially the same manner, and can provide the same effects as those of the semiconductor device not having such an AlN layer between the substrate and the buffer layer.

[0076] As described hereinabove, a semiconductor device according to one embodiment of the present invention includes an AlGaN separating layer having a low AlN composition ratio between a GaN channel layer and a GaN buffer layer. With such a structure, a leakage current between a source and a drain, a gate leakage current, and a leakage current between

devices caused by residual carriers unintentionally caused in the GaN layers (channel layer) are significantly reduced, while electrons are efficiently confined in the channel layer, whereby the gate length can be easily decreased, and accordingly, device properties can be improved.

[0077] Another embodiment of the present invention provides a double-doped, GaN-based heterostructure FET having a novel structure in which electrons can accumulate so as to form a single electron channel. Such a structure provides a superior mutual conductance and a high current driving performance, and contributes to the improvement in power characteristics of a gallium nitride-based semiconductor device. Furthermore, with such a structure, the gate length can be easily decreased, and accordingly, the device properties can be improved.

[0078] Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.

Claims

What is claimed is:

1. A semiconductor device comprising:
a substrate;
a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of Ga atoms;
a separating layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the buffer layer, wherein surfaces of the separating layer are c facets of In, Al, or Ga atoms;
a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the separating layer, wherein surfaces of the channel layer are c facets of Ga or In atoms; and
an electron supply layer including AlGaN formed on the channel layer, wherein surfaces of the electron supply layer are c facets of Al or Ga atoms,
wherein the AlN composition ratio in the separating layer is smaller than the AlN composition ratio in the electron supply layer.

2. A semiconductor device according to claim 1, wherein, in the separating layer including (InXAl1-X)YGa1-YN, X=0.

3. A semiconductor device according to claim 2, wherein the AlN composition ratio in the separating layer is equal to or smaller than about 0.1.

4. A semiconductor device according to claim 2, wherein the AlN composition ratio in the separating layer gradually increases from an interface with the buffer layer to an interface with the electron supply layer.

5. A semiconductor device comprising:
a substrate;
a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of Ga atoms;
a first electron supply layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the buffer layer, wherein surfaces of the first electron supply layer are c facets of In, Al, or Ga atoms;
a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the first electron supply layer, wherein surfaces of the channel layer are c facets of Ga or In atoms; and
a second electron supply layer including AlGaN formed on the channel layer, wherein surfaces of the electron supply layer are c facets of Al or Ga atoms,
wherein the AlN composition ratio, the InN composition ratio, and the GaN composition ratio in the first electron supply layer are set such that electrons accumulate in a vicinity of a heterointerface between the first electron supply layer and the channel layer due to a variation in polarization.

6. A semiconductor device comprising:
a substrate;
a buffer layer including GaN formed on the substrate, wherein surfaces of the buffer layer are c facets of N atoms;
a first electron supply layer including AlGaN formed on the buffer layer, wherein surfaces of the first electron supply layer are c facets of N atoms;
a channel layer including GaN, InGaN, or a combination of GaN and InGaN formed on the first electron supply layer, wherein surfaces of the channel layer are c facets of N atoms; and
a second electron supply layer including (InXAl1-X)YGa1-YN (where 0<=X<=1, 0<=Y<=1) formed on the channel layer, wherein surfaces of the electron supply layer are c facets of N atoms,
wherein the AlN composition ratio, the InN composition ratio, and the GaN composition ratio in the first electron supply layer are set such that electrons accumulate in a vicinity of a heterointerface between the second electron supply layer and the channel layer due to a variation in polarization.

FIG. 1A

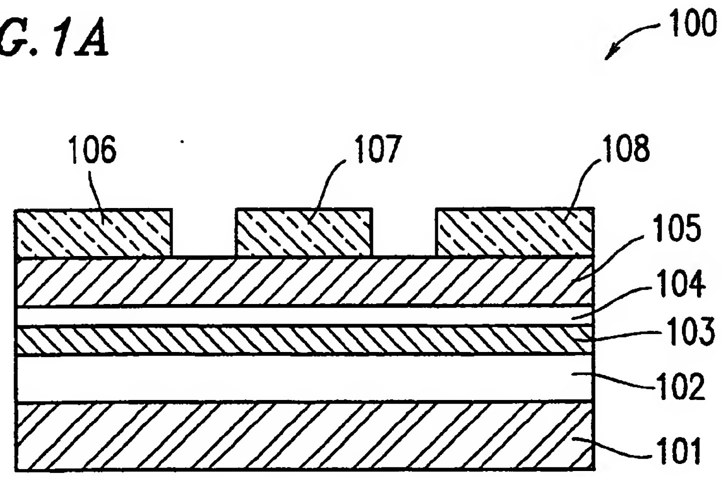

100
106
107
108
105
104
103
102
101

FIG. 1B

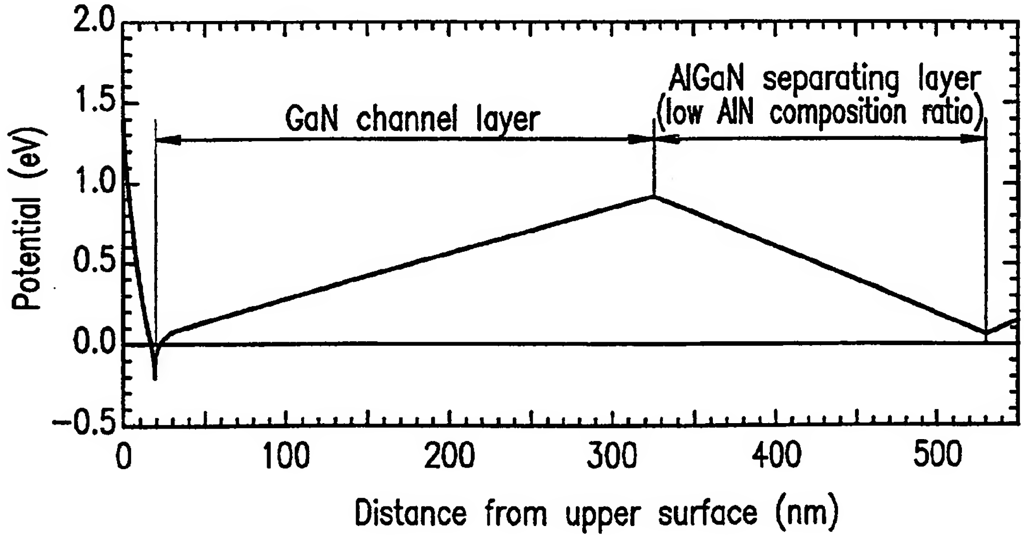
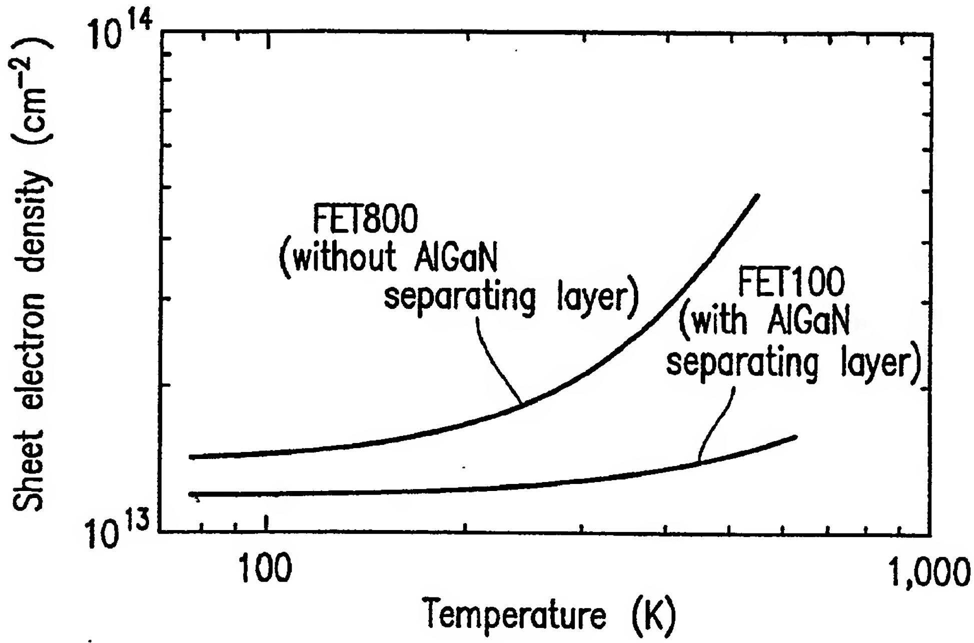

2.0
1.5
1.0
0.5
0.0
−0.5
Potential (eV)
GaN channel layer
AlGaN separating layer
(low AlN composition ratio)
0
100
200
300
400
500
Distance from upper surface (nm)

FIG.2



10^{14}
10^{13}
Sheet electron density (cm^{-2})
FET800
(without AlGaN
separating layer)
FET100
(with AlGaN
separating layer)
100
1,000
Temperature (K)

FIG. 3A

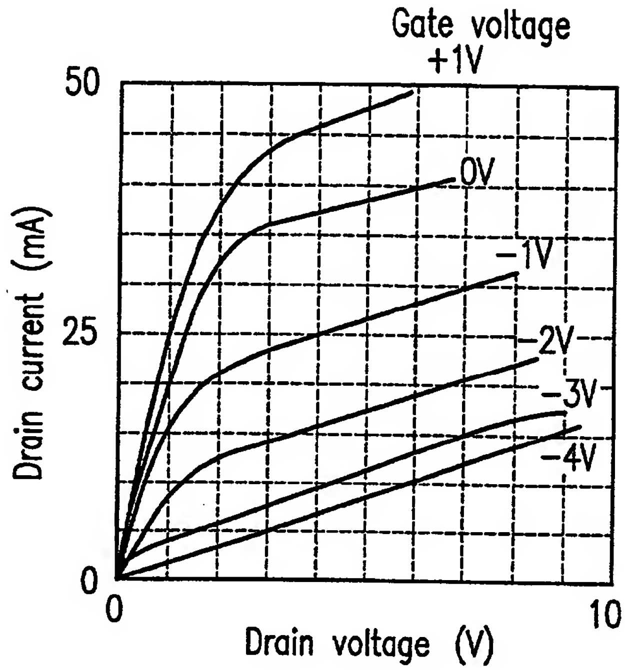

Gate voltage
+1V
0V
−1V
−2V
−3V
−4V
50
25
0
0
10
Drain current (mA)
Drain voltage (V)

FIG. 3B

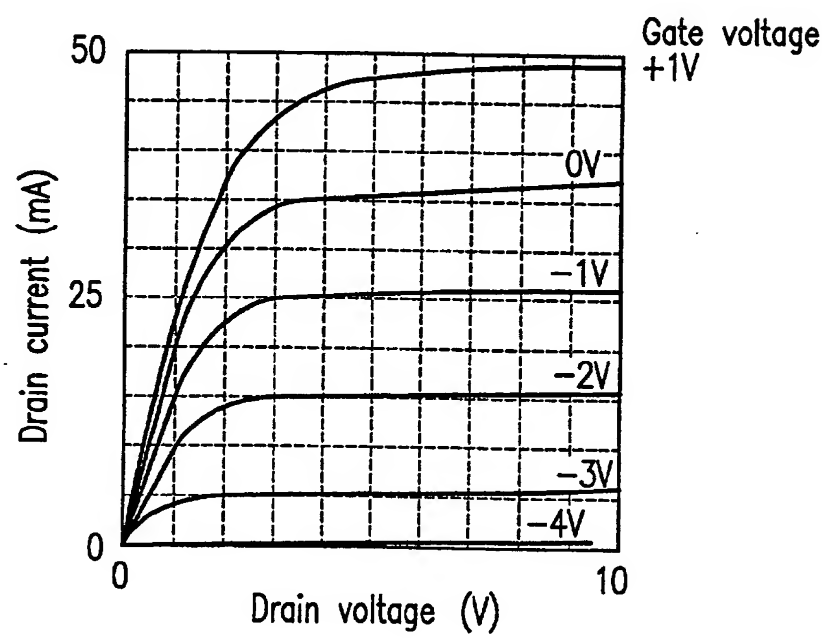

Gate voltage
+1V
0V
−1V
−2V
−3V
−4V
50
25
0
0
10
Drain current (mA)
Drain voltage (V)

FIG. 4

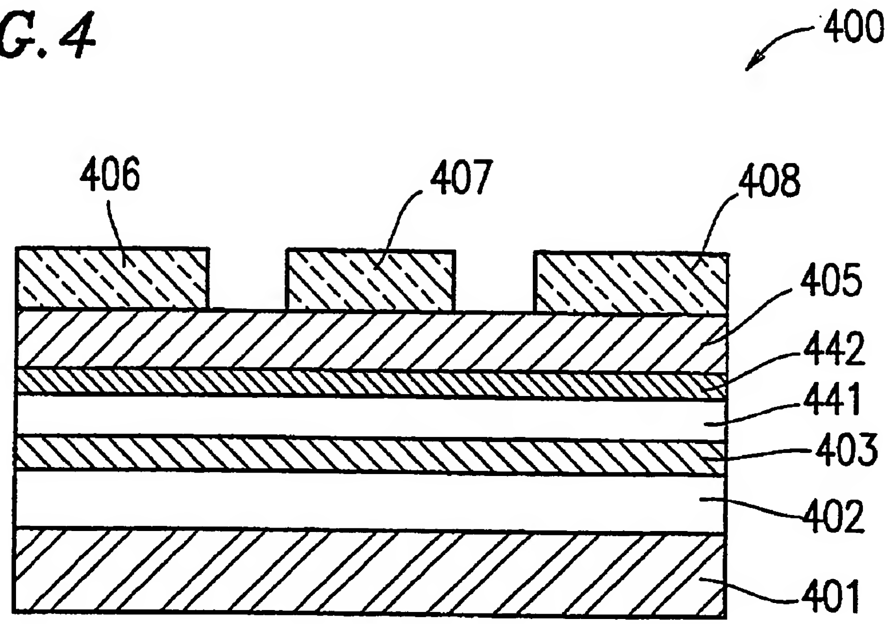

400
406
407
408
405
442
441
403
402
401

FIG. 5

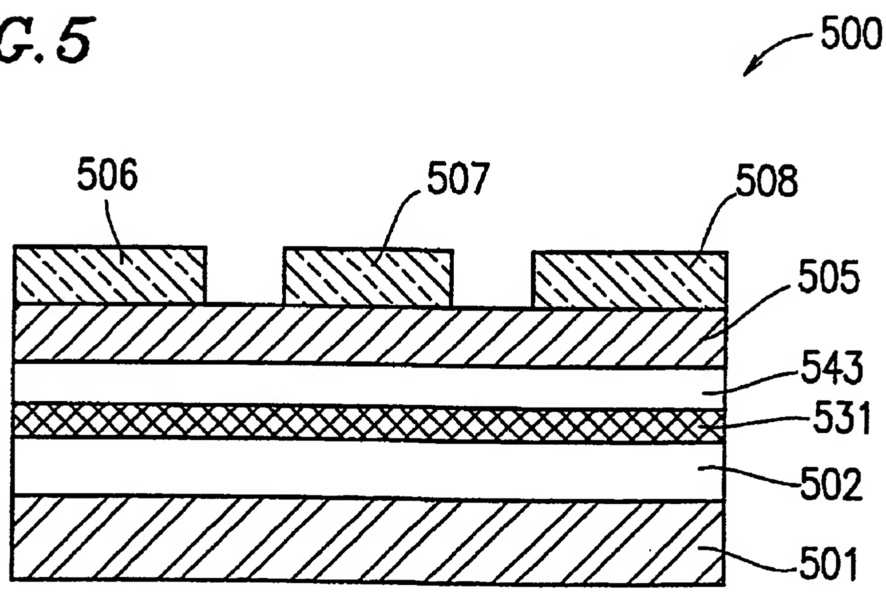

500
506
507
508
505
543
531
502
501

FIG. 6

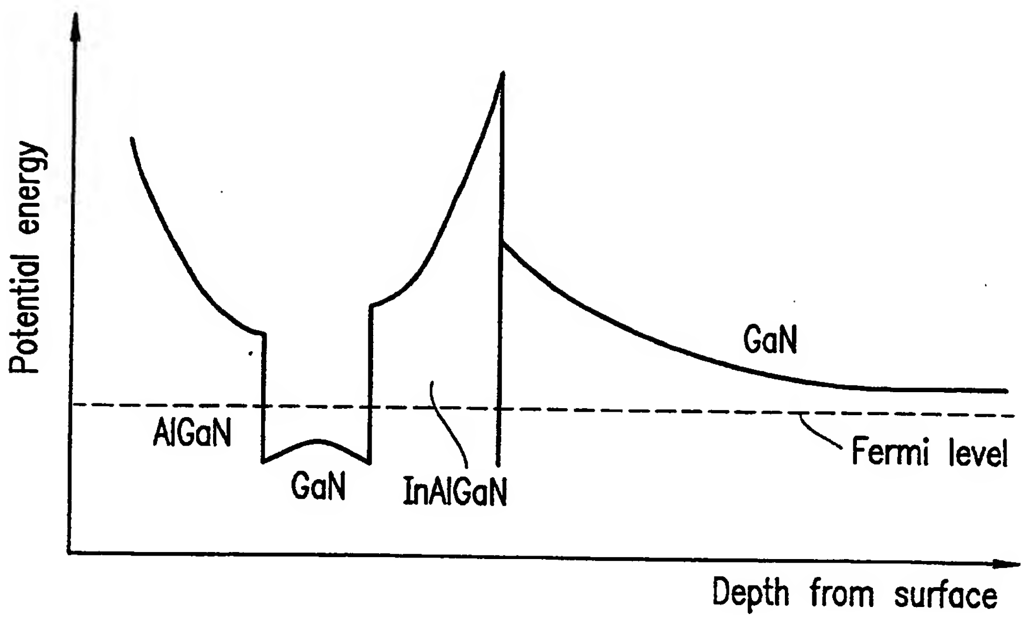

Potential energy
GaN
AlGaN
GaN
InAlGaN
Fermi level
Depth from surface

FIG. 7A

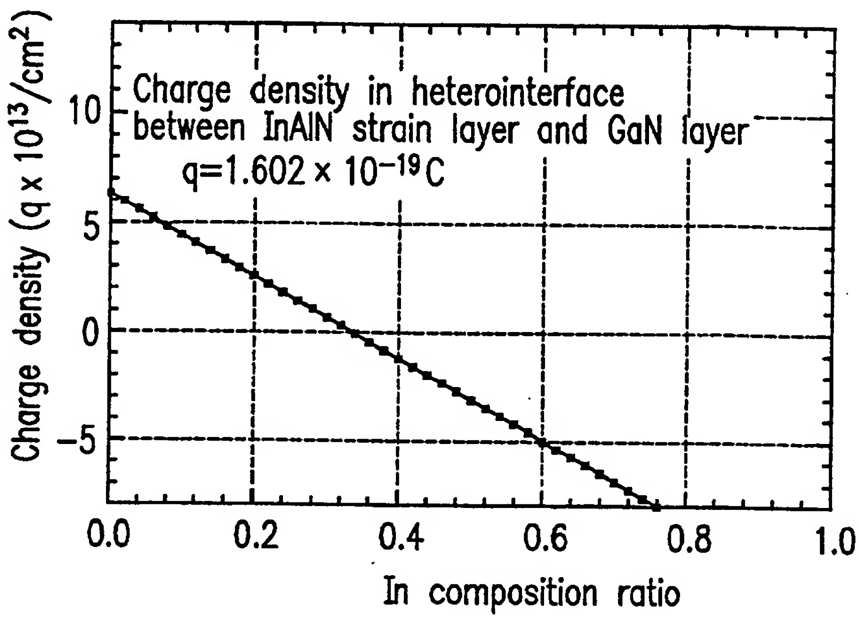

Charge density in heterointerface between InAlN strain layer and GaN layer
q=1.602 × 10⁻¹⁹C
Charge density (q x 10¹³/cm²)
10
5
0
−5
0.0
0.2
0.4
0.6
0.8
1.0
In composition ratio

FIG. 7B

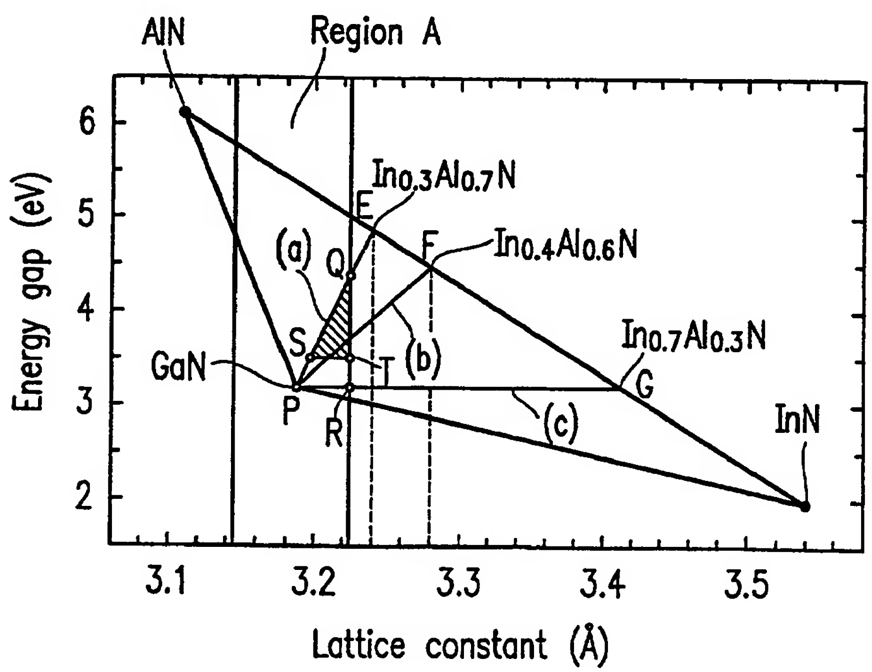

AlN
Region A
In0.3Al0.7N
In0.4Al0.6N
In0.7Al0.3N
InN
GaN
E
F
G
Q
S
T
P
R
(a)
(b)
(c)
Energy gap (eV)
6
5
4
3
2
3.1
3.2
3.3
3.4
3.5
Lattice constant (Å)

FIG. 8

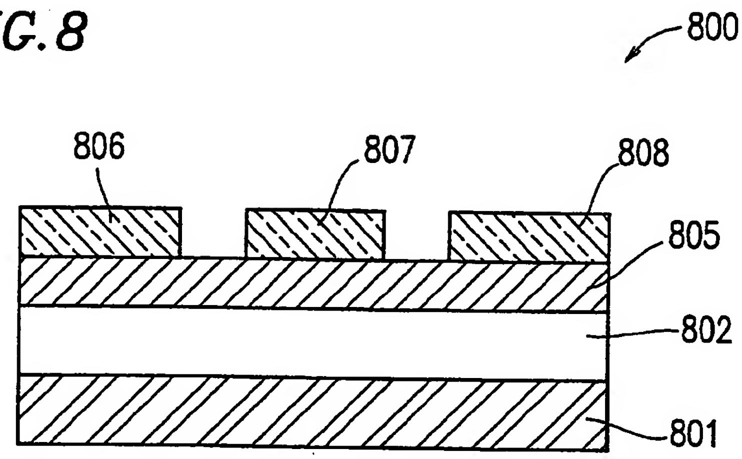


FIG. 9

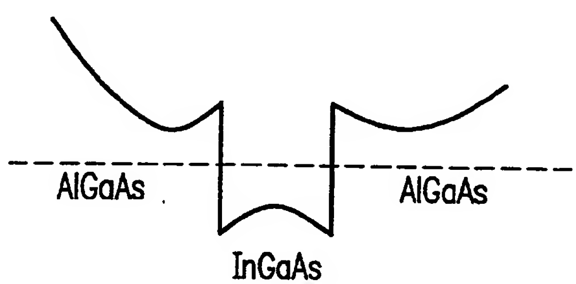


FIG. 10

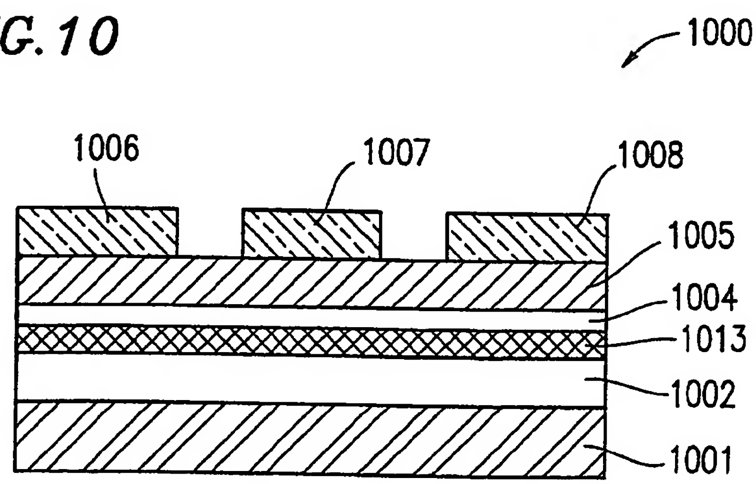
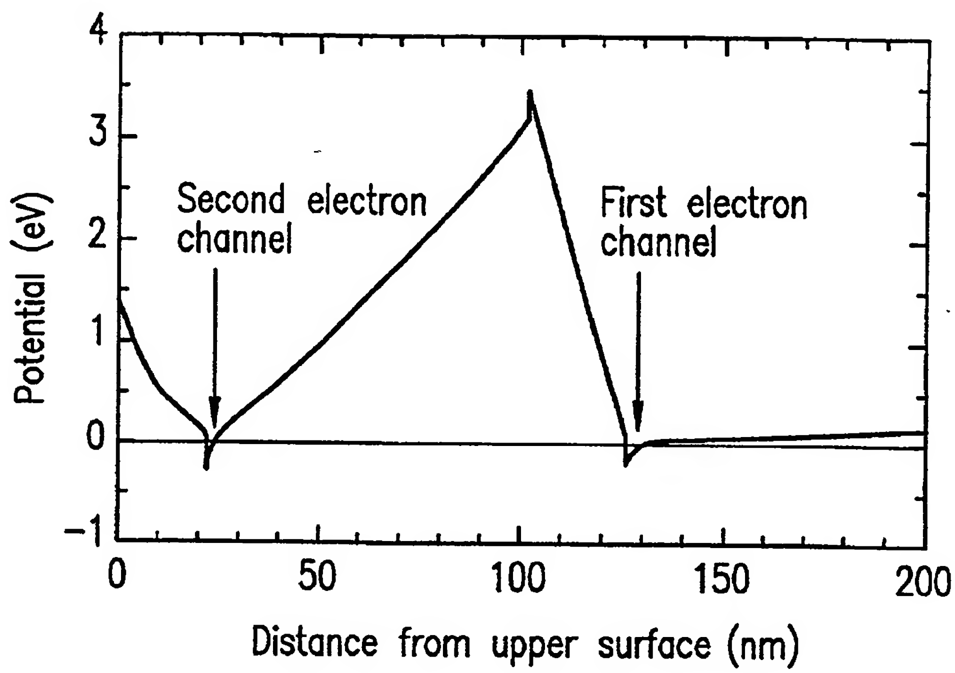


FIG. 11



4
3
2
1
0
−1
Potential (eV)
Second electron channel
First electron channel
0
50
100
150
200
Distance from upper surface (nm)